



SGM4064

Over-Voltage Protection IC and Li+ Charger Front-End Protection IC with LDO Mode

GENERAL DESCRIPTION

The SGM4064 is a charger front-end integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuitry. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.1V output with input voltages up to the input over-voltage threshold ($V_{OVP} = 6.8V$). During input over-voltage conditions, the IC immediately turns off the internal pass FET disconnecting the charging circuitry from the damaging input source. Additionally, if the battery voltage rises to unsafe levels while charging, power is removed from the system. The IC also monitors its die temperature and switches off if it exceeds $145^{\circ}C$. When the IC is controlled by a processor, the IC provides status information about fault conditions to the host.

The SGM4064 is available in Green TDFN-2x2-8L package and is rated over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.

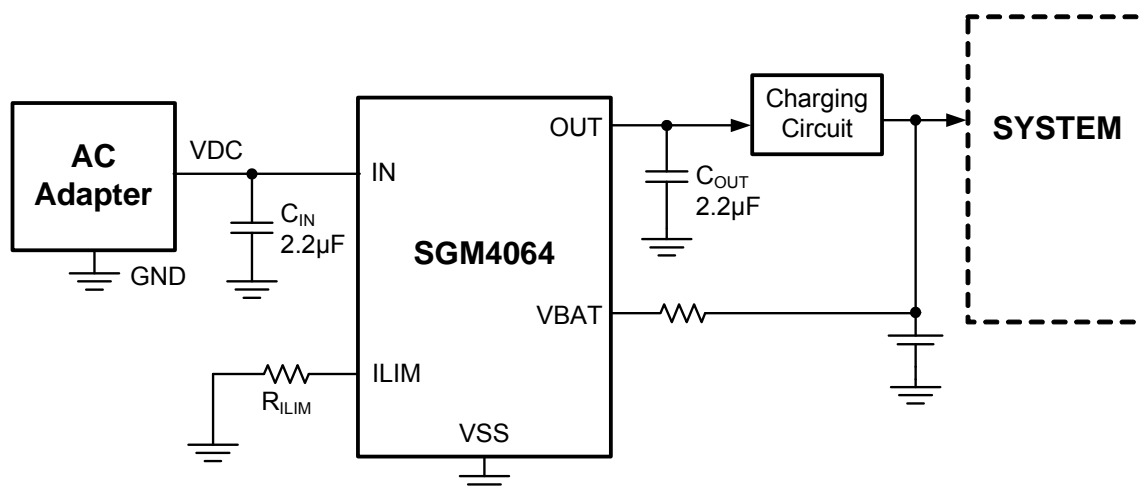
FEATURES

- Input Over-Voltage Protection
- Accurate Battery Over-Voltage Protection
- Soft-Start to Prevent Inrush Currents
- Soft-Stop to Prevent Voltage Spikes
- 18V Maximum Input Voltage
- Supports up to 1.5A Load Current
- Thermal Shutdown
- Enable Function
- Fault Status Indication
- Available in Green TDFN-2x2-8L Package

APPLICATIONS

Smart Phones, Mobile Phones
PDAs
MP3 Players
Low-Power Handheld Devices

APPLICATION SCHEMATIC



SGM4064

Over-Voltage Protection IC and Li+ Charger Front-End Protection IC with LDO Mode

PACKAGE/ORDERING INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	MARKING INFORMATION	PACKING OPTION
SGM4064	SGM4064YDE8G/TR	TDFN-2×2-8L	-40°C to +85°C	4064 XXXX	Tape and Reel, 3000

NOTE: XXXX = Date Code.

ABSOLUTE MAXIMUM RATINGS

IN (with respect to VSS).....-0.3V to 28V
OUT (with respect to VSS).....-0.3V to MIN ($V_{IN} + 0.3V$, 6V)
ILIM, FAULT, CE, VBAT (with respect to VSS)-0.3V to 6V
Output Source Current (OUT Pin).....2A
Output Sink Current (FAULT Pin)15mA
Package Thermal Resistance
TDFN-2×2-8L, θ_{JA}75°C/W
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....150°C
Operating Temperature Range.....-40°C to +85°C
Lead Temperature (Soldering 10 sec)..... 260°C
ESD Susceptibility
HBM.....4000V
MM.....200V

NOTE:

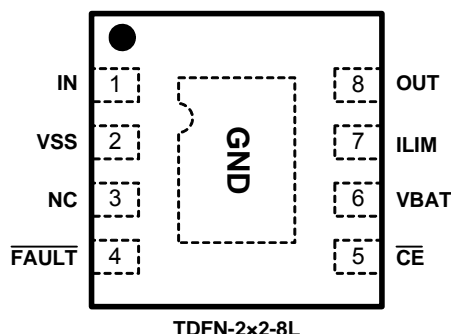
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN	Input Power. Connected to external DC supply. Bypass IN to VSS with a ceramic capacitor (1μF MIN).
2	VSS	Ground Terminal. Connect to the thermal pad and to the ground rail of the circuit.
3	NC	Do not connect to any external circuit.
4	$\overline{\text{FAULT}}$	Open-drain Device Status Output. $\overline{\text{FAULT}}$ is pulled to VSS internally when the input pass FET has been turned off due to input over-voltage or overload current protection, an over-temperature condition, or because the battery voltage is outside safe limits. $\overline{\text{FAULT}}$ is high impedance during normal operation.
5	$\overline{\text{CE}}$	Active-Low Chip Enable Input. Connect $\overline{\text{CE}}$ = "HIGH" to turn the input pass FET off. Connect $\overline{\text{CE}}$ = "LOW" to turn the internal pass FET on, connecting the input to the charging circuitry. $\overline{\text{CE}}$ is internally pulled down and pull-down resistor is about 200kΩ.
6	VBAT	Battery Voltage Sense Input. Connected to pack positive terminal through a 10kΩ resistor.
7	ILIM	Overload Current Protection Programming Pin. Connect a resistor to VSS to set the overload current protection threshold: $I_{\text{OCP}} = 200 / (25 + R_{\text{ILIM}})$ (current in A, resistance in kΩ)
8	OUT	Output Terminal to the Charging System. Bypass OUT to VSS with a ceramic capacitor (2.2μF MIN).
Exposed Pad	GND	The thermal pad is electrically connected to VSS internally. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
IN Voltage Range	V_I	3.3	18	V
Current, OUT Pin	I_O		1.5	A

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, R_{LIM} = 100kΩ, \overline{CE} = LOW, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
Under-Voltage Lockout, Input Power Detected Threshold	UVLO	V _{IN} = 0V to 3V	2.5	2.65	2.8	V
Hysteresis on UVLO	V _{hys(UVLO)}	V _{IN} = 3V to 0V		225		mV
Deglitch Time, Input Power Detected Status	t _{DGL(PGOOD)}	Time measured from V _{IN} = 0V to 5V, 1μs rise-time		9		ms
Operating Current	I _{DD}	V _{IN} = 5V, no load on OUT pin		185	260	μA
Standby Current	I _{STDBY}	\overline{CE} = HIGH, V _{IN} = 5.5V		0.5	2	μA
INPUT-TO-OUTPUT CHARACTERISTICS						
Q1 Off-State Leakage Current	I _{OFF}	\overline{CE} = HIGH, V _{IN} = 5.5V			5	μA
Dropout Voltage IN to OUT	V _{DO}	V _{IN} = 5V, I _{OUT} = 0.5A		120	170	mV
INPUT OVER-VOLTAGE PROTECTION						
Output Voltage	V _{O(REG)}	V _{IN} = 5.5 to V _{OVP} - V _{hys(OVP)} , no load on OUT pin	4.9	5.1	5.3	V
Input Over-Voltage Protection Threshold	V _{OVP}		6.35	6.8	7.05	V
Hysteresis on OVP	V _{hys(OVP)}		50	120	280	mV
Input Over-Voltage Protection Propagation Delay ⁽¹⁾	t _{PD(OVP)}	V _{IN} = 6V to 9V		200		ns
Recovery Time from Input Over-Voltage Condition	t _{REC(OVP)}	Time measured from V _{IN} = 9V to 6V, 1μs fall-time		9		ms
BATTERY OVER-VOLTAGE PROTECTION						
Battery Over-Voltage Protection Threshold	BV _{OVP}	V _{OVP} - V _{hys(OVP)} > V _{IN} > 4.5V	4.275	4.35	4.41	V
Hysteresis on BV _{OVP}	V _{hys(BVovp)}	V _{OVP} - V _{hys(OVP)} > V _{IN} > 4.5V	190	255	320	mV
Input Bias Current on VBAT Pin	I _{VBAT}			20	180	nA
Deglitch Time, Battery Over-Voltage Detected	t _{DGL(BVovp)}	V _{IN} > 4.5V, time measured from V _{VBAT} rising from 4.1V to 4.5V to \overline{FAULT} going low		180		μs
THERMAL PROTECTION						
Thermal Shutdown Temperature	T _{J(OFF)}			145		°C
Thermal Shutdown Hysteresis	T _{J(OFF-HYS)}			15		°C
LOGIC LEVELS ON \overline{CE}						
Logic LOW Input Voltage	V _{IL}				0.4	V
Logic HIGH Input Voltage	V _{IH}		1.4			V
Input LOW Current	I _{IL}			0.3	1.5	μA
Input HIGH Current	I _{IH}	V \overline{CE} = 1.8V		9	15	μA
LOGIC LEVELS ON \overline{FAULT}						
Output LOW Voltage	V _{OL}	I _{SINK} = 5mA		0.14	0.3	V
Off-State Leakage Current, HI-Z	I _{IKg}	V \overline{FAULT} = 5V		0.01	25	μA

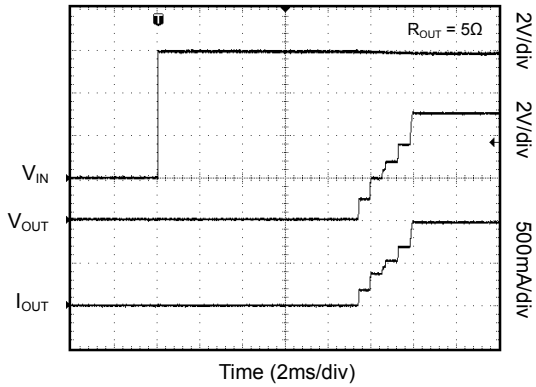
NOTE:

1. Not tested. Specified by design.

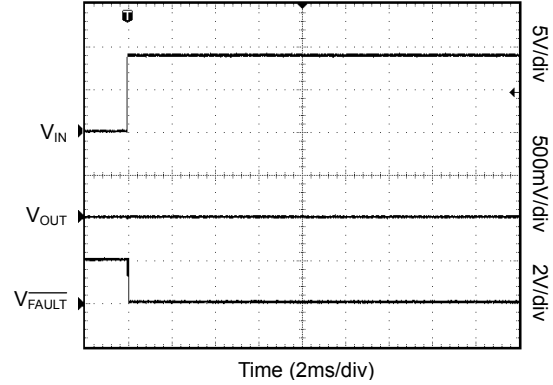
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $C_{IN} = C_{OUT} = 2.2\mu\text{F}$, $R_{ILIM} = 100\text{k}\Omega$, unless otherwise noted.

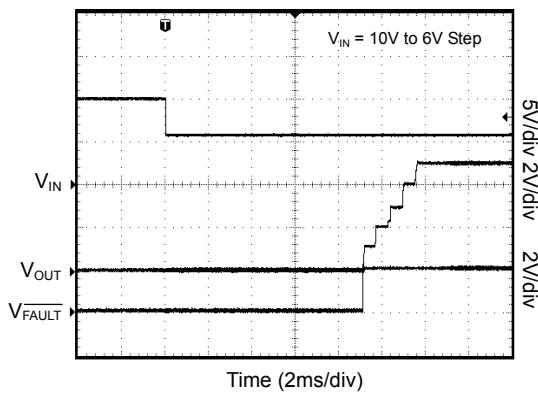
Normal Power-On Showing Soft-Start



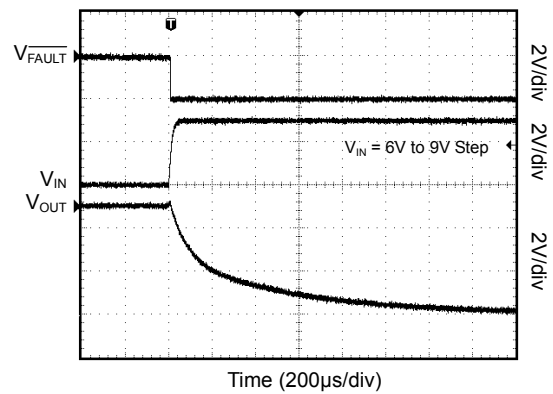
OVP at Power-On



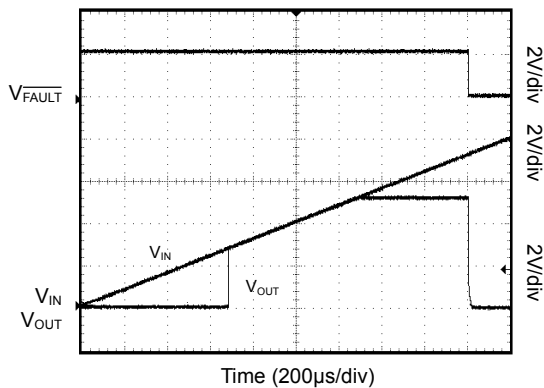
Recovery from OVP



OVP Response for Input Step



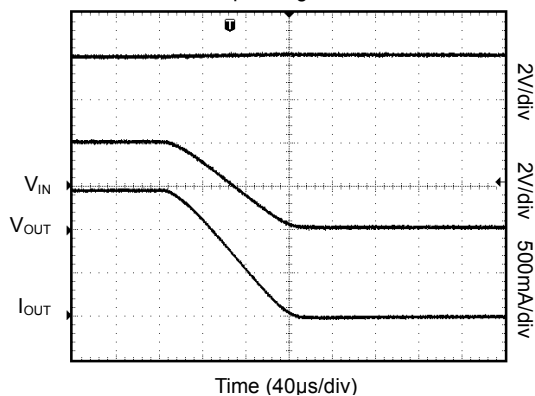
Slow Input Ramp into OVP Event



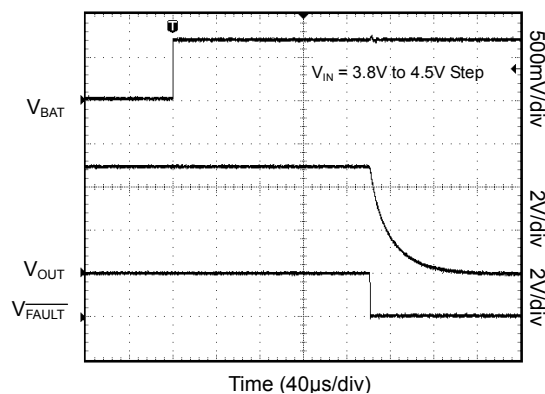
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $C_{IN} = C_{OUT} = 2.2\mu\text{F}$, $R_{ILIM} = 100\text{k}\Omega$, unless otherwise noted.

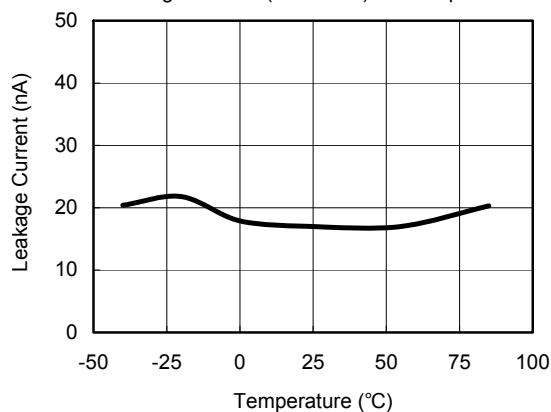
Soft-Stop during OCP Event



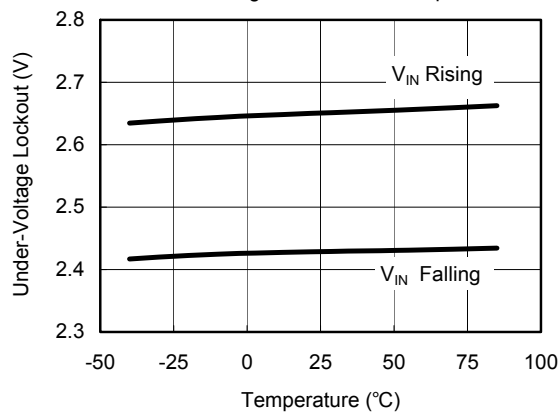
Battery OVP Event



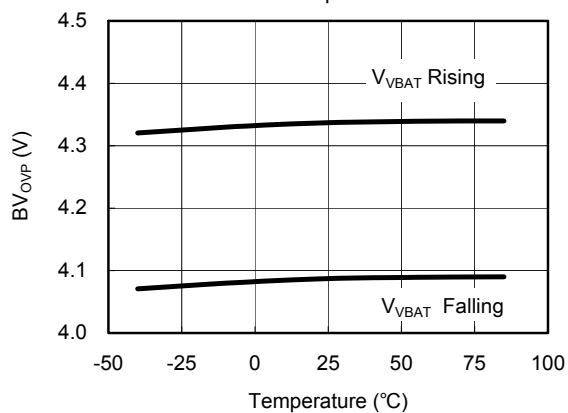
Leakage Current (VBAT Pin) vs. Temperature



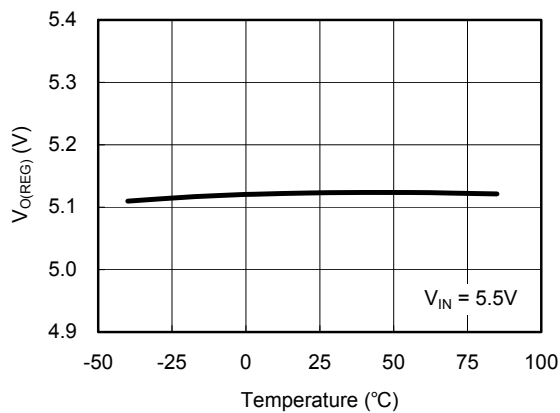
Under-Voltage Lockout vs. Temperature



Battery Over-Voltage Protection Threshold vs. Temperature

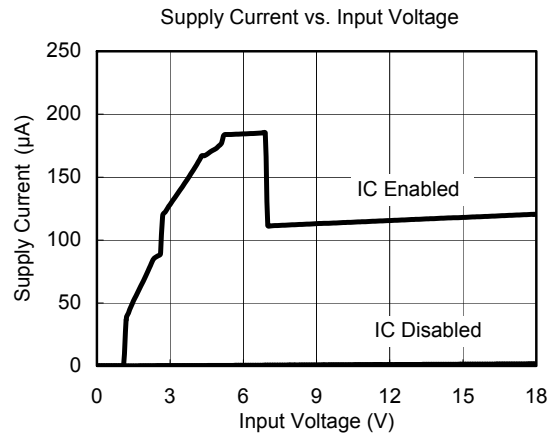
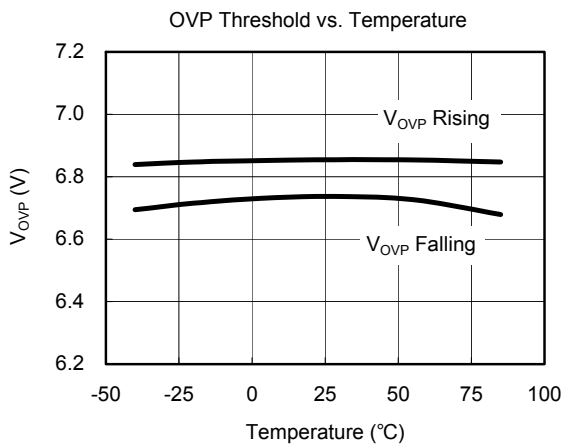


Output Voltage Regulation vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, C_{IN} = C_{OUT} = 2.2μF, R_{ILIM} = 100kΩ, unless otherwise noted.



TYPICAL APPLICATION CIRCUIT

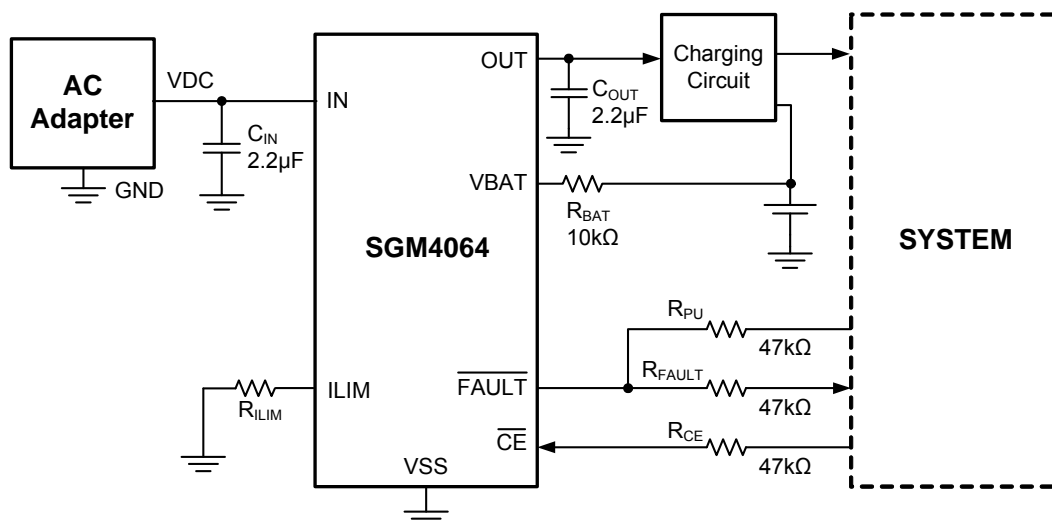


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

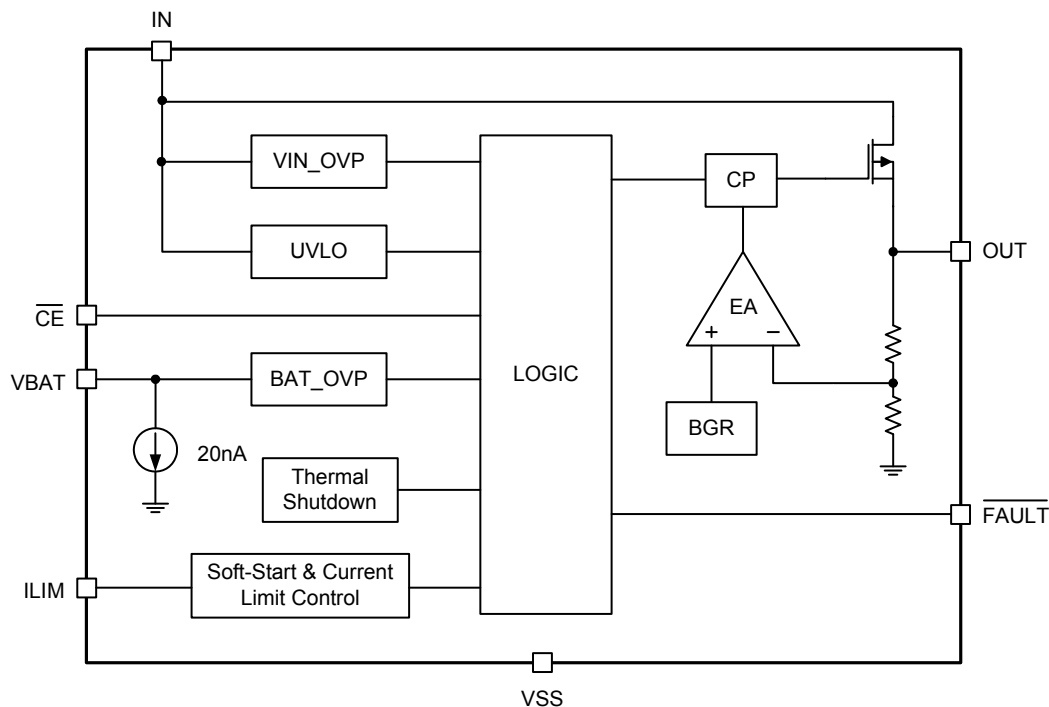
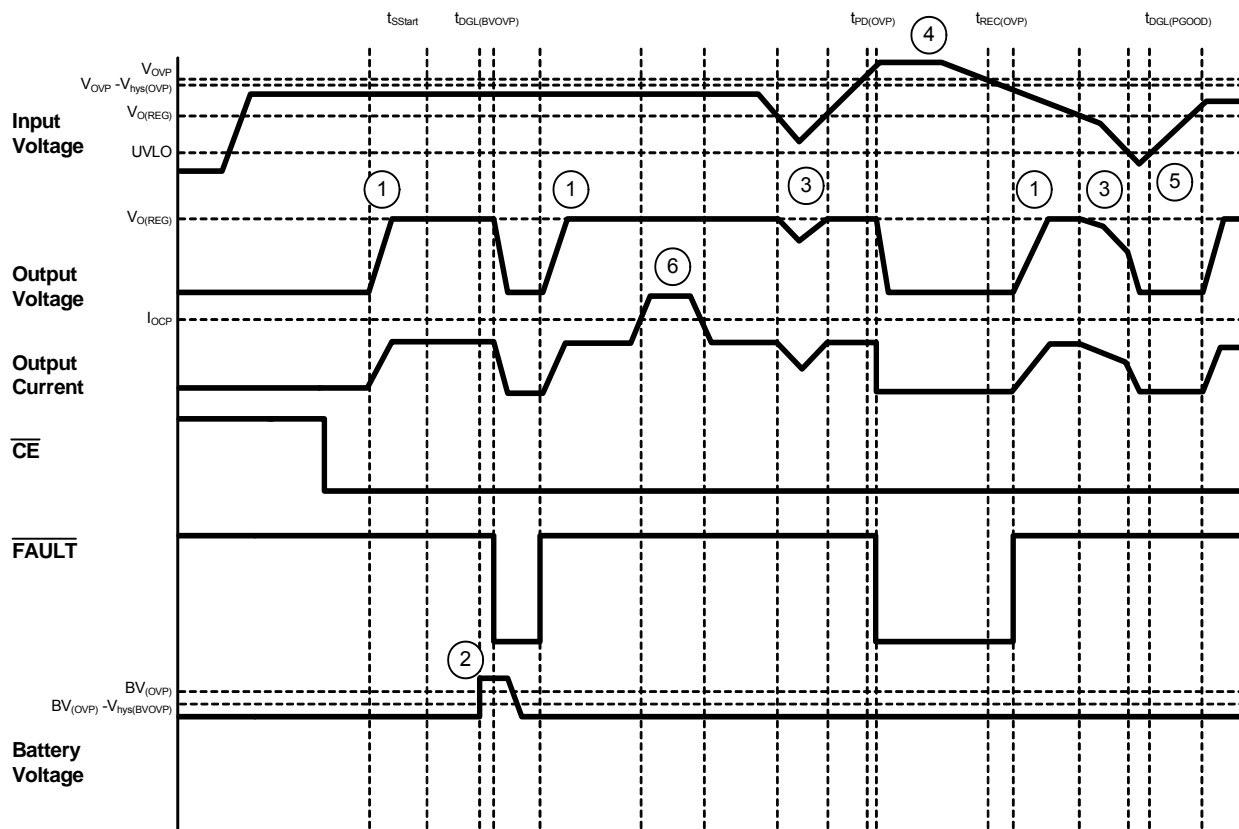


Figure 2. Functional Block Diagram

TIMING DIAGRAM



1. Normal start-up condition
2. Battery over-voltage event
3. $V_{UVLO} < V_{IN} < V_{O(REG)}$, V_{OUT} tracks V_{IN}
4. Input over-voltage event
5. Input below $UVLO$
6. High-current event during normal operation

Figure 3. Timing Diagram

DETAILED FUNCTIONAL DESCRIPTION

The SGM4064 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit and the input source. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.1V output with input voltages up to the input over-voltage threshold ($V_{OVP} = 6.8V$). If the input voltage exceeds V_{OVP} , the IC shuts off the pass FET and disconnects the system from input power. Additionally, if the battery voltage rises above 4.35V, the IC switches off the pass FET, removing the power from the system until the battery voltage falls to safe levels. The IC also monitors its die temperature and switches the pass FET off if it exceeds 145°C.

The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

Power-On

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. During power-on reset, the IC waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are within operation limits, the pass FET is turned on. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input due to the resonant circuit formed by the parasitic inductance of the adapter cable and the input bypass capacitor. During the soft-start time, t_{SStart} , the output current is increased in several steps. Each step is 625μs.

Power-Down

The device remains in power-down mode when the input voltage at the IN pin is below the under-voltage threshold (UVLO) of 2.65V. The FET connected between the IN and OUT pins is off, and the status output, \overline{FAULT} , is set to high impedance.

Start-Up Overload Current Protection

During start-up, if the eight soft-start steps are completed and the output current exceeds overload current protection (OCP), the IC initiates an OCP check timer ($t_{CHK(OCP)}$). During this check, the output current is clamped to the OCP threshold (I_{OCP}). I_{OCP} is programmed by a resistor R_{ILIM} connected from the ILIM pin to VSS, and can be calculated from the following equation:

$$I_{OCP} = 200 / (25 + R_{ILIM}) \text{ (current in A, resistance in k}\Omega\text{)}$$

For example, $I_{OCP} = 1.6A$ if $R_{ILIM} = 100k\Omega$.

If the 5ms $t_{CHK(OCP)}$ timer expires and the output current remains clamped by I_{OCP} , the internal pass FET is turned off using the soft-stop method, \overline{FAULT} is pulled low and the $t_{REC(OCP)}$ timer begins. Once the $t_{REC(OCP)}$ timer expires, \overline{FAULT} becomes high impedance and the soft-start sequence restarts. The device repeats the start/fail sequence until the overload condition is removed. Once the overload condition is removed, the OCP circuitry is disabled and the device enters normal operation. At high temperature this overload current protection during start-up may not be working well.

DETAILED FUNCTIONAL DESCRIPTION

The device continuously monitors the input voltage and the battery voltage as described in detail below:

Input Over-Voltage Protection

The output voltage at OUT pin of the SGM4064 operates similarly to a linear regulator. While the input voltage is less than $V_{O(REG)}$, and above the UVLO, the output voltage tracks the input voltage (less the drop caused by $R_{DS(on)}$ of the pass FET). When the input voltage is greater than $V_{O(REG)}$ (plus the $R_{DS(on)}$ drop) and less than V_{OVP} , the output voltage is regulated to $V_{O(REG)}$. $V_{O(REG)}$ is 5.1V for the SGM4064. If the input voltage is increased above V_{OVP} , the internal pass FET is turned off, removing power from the charging circuitry connected to OUT. The \overline{FAULT} output is then asserted low. When the input voltage drops below $V_{OVP} - V_{hys(OVP)}$ (but is still above UVLO), the pass FET is turned on after a deglitch time of $t_{REC(OVP)}$. The deglitch time ensures that the input supply has stabilized.

Battery Over-Voltage Protection

The battery over-voltage threshold BV_{OVP} is internally set to 4.35V for the SGM4064. If the battery voltage exceeds the BV_{OVP} threshold for longer than $t_{DGL(BV_{OVP})}$, the pass FET is turned off (using soft-stop), and \overline{FAULT} is asserted low. The pass FET is turned on (using the soft-start sequence) once the battery voltage drops to $BV_{OVP} - V_{hys(BV_{OVP})}$.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the pass FET is turned off, and the \overline{FAULT} output is asserted low. The FET is turned on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which is used to enable and disable the device. Connect the \overline{CE} pin high to turn off the internal pass FET. Connect the \overline{CE} pin low to turn on the internal pass FET and enter the start-up routine. The \overline{CE} pin has an internal pull-down resistor and can be left unconnected. The \overline{FAULT} pin is high impedance when the \overline{CE} pin is high.

Fault Indication

The \overline{FAULT} pin is an active-low, open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting \overline{CE} high. With \overline{CE} low, the \overline{FAULT} pin goes low whenever any of these events occurs:

1. Input over-voltage
2. Battery over-voltage
3. IC over-temperature

See Figure 3 for an example of \overline{FAULT} conditions during these events. Connect the \overline{FAULT} pin to the desired logic level voltage rail through a resistor between 1k Ω and 50k Ω .

APPLICATION INFORMATION

Selection of R_{BAT}

It is recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 18V, and applying 18V to the battery may cause failure of the device and can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in the event of failure. For safety, R_{BAT} must have a high value. The problem with a large R_{BAT} is that the voltage drops across the resistor because of the VBAT bias current, I_{VBAT} , which causes an error in the BV_{OVP} threshold. This error might be over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range of 10k Ω to 100k Ω is a good compromise. If the IC fails with R_{BAT} equal to 10k Ω , the maximum current flowing into the battery would be $(18V - 3V)/10k\Omega = 1500\mu A$, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 10k Ω results in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} \approx 1.7mV$. This is negligible compared to the internal tolerance of 60mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin can either be connected to VSS or left floating.

Selection of R_{CE}

The \overline{CE} pin can be used to enable and disable the IC. If host control is not required, the \overline{CE} pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the \overline{CE} pin can be controlled by a host processor. As with the VBAT pin (see previous discussion), the \overline{CE} pin must be connected to the host GPIO pin through as large a resistor as possible. The drop across the resistor is given by $R_{CE} \times I_{IH}$ and the limitation of R_{CE} is calculated by equation:

$$V_{OH} - R_{CE} \times I_{IH} > V_{IH}$$

V_{OH} is the high level output voltage from host I/O.

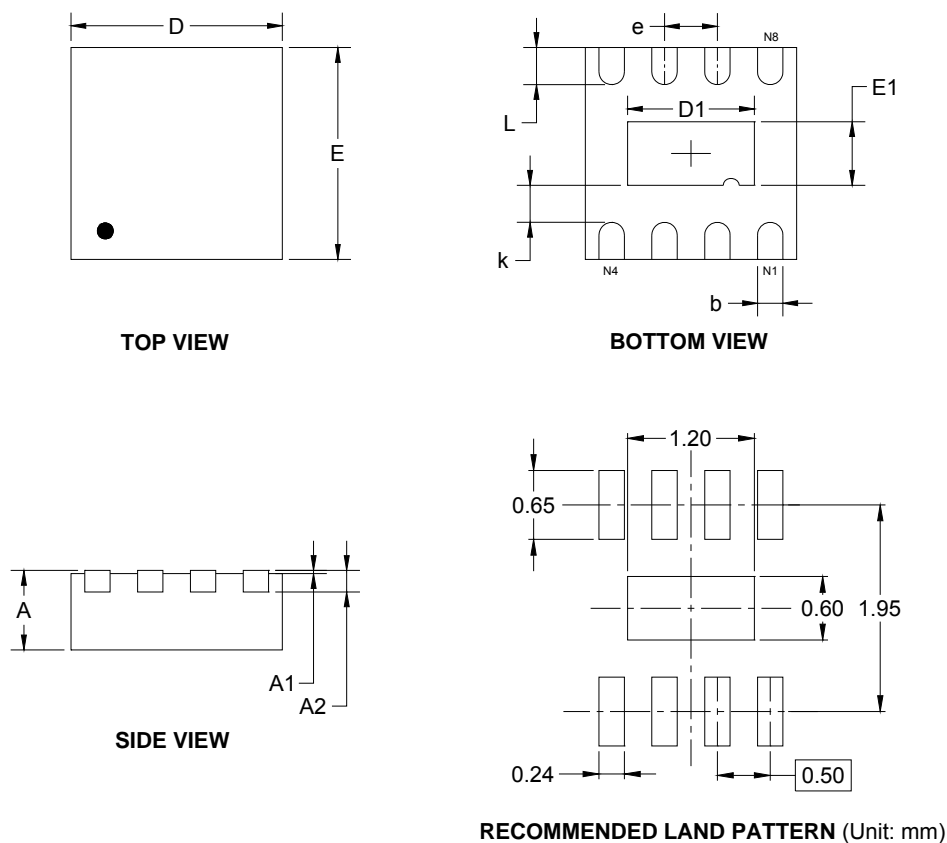
Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 1 is for decoupling and serves an important purpose. Whenever a step change downwards in the system load current occurs, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1 μF be used at the input of the device. It must be located in close proximity to the IN pin.

C_{OUT} in Figure 1 is also important. During an over-voltage transient, this capacitance limits the output overshoot until the power FET is turned off by the over-voltage protection circuitry. C_{OUT} must be a ceramic capacitor of at least 2.2 μF , located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

PACKAGE OUTLINE DIMENSIONS

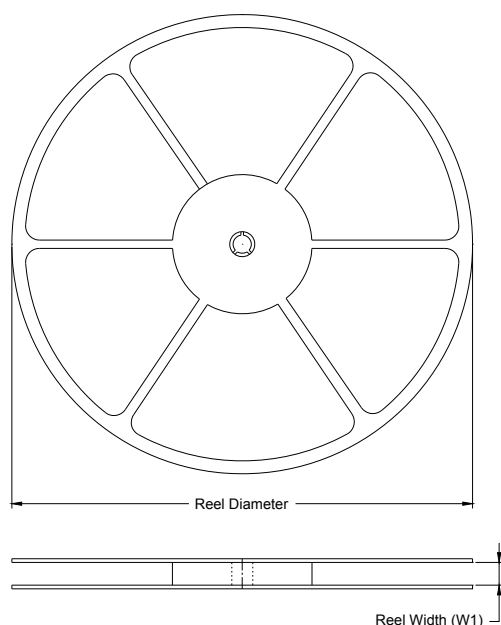
TDFN-2x2-8L



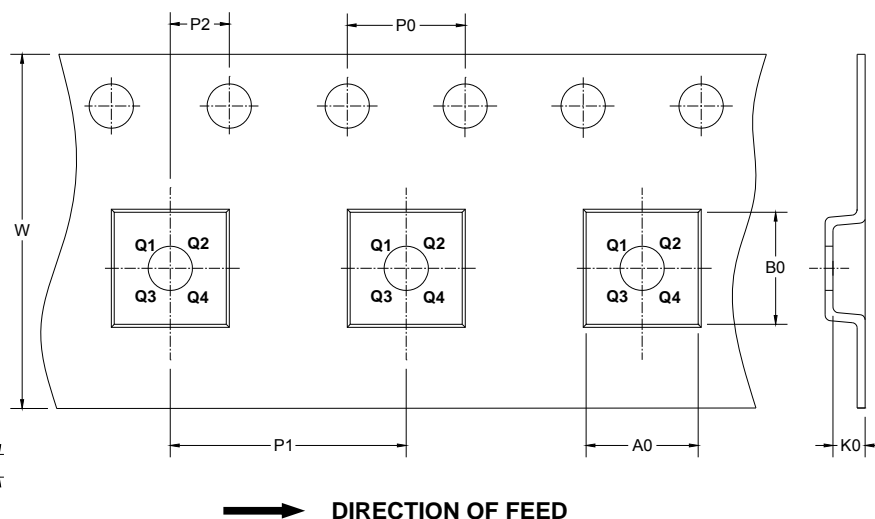
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018

TAPE AND REEL INFORMATION

REEL DIMENSIONS



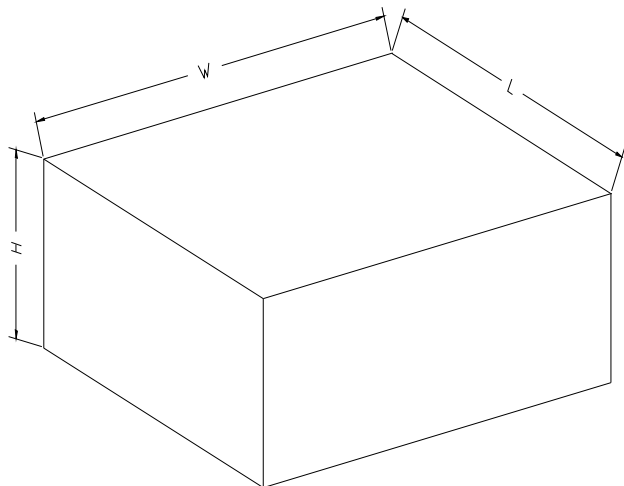
TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8L	7"	9.5	2.30	2.30	1.10	4.00	4.00	2.00	8.00	Q1

CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18