SGM61230



4.5V to 28V Input, 3A Output,

Synchronous Step-Down Converter

GENERAL DESCRIPTION

The SGM61230 is step-down converter with 4.5V to 28V input range and 3A rated output current. It is an easy to use device with power switches and current mode control compensation all integrated in a small 6-pin package. A 5ms soft-start is also included to minimize the inrush current and BOM.

This device features cycle by cycle current limiting, thermal shutdown with auto recovery and output overvoltage protection. The current limiting is implemented for both switches and has foldback feature to prevent overheating (and thermal shutdown) when an output short is detected. Automatic recovery after over-current, output short, overheating or over-voltage faults maintains the system operational with no shutdown.

This converter has a fixed 400kHz switching frequency that minimizes the EMI noise problems. However the actual frequency drops during PSM (pulse skip mode) to maximize efficiency at light load. It also drops in some fault conditions.

SGM61230 is available in a Green TSOT-23-6 package and can operates over a wide ambient temperature range of -40°C to +125°C.

FEATURES

- Wide 4.5V to 28V Input Voltage Range
- **3A Continuous Output Current**
- Integrated 70mΩ/39mΩ Power MOSFETs
- 3µA Shutdown Current
- 30µA Quiescent Current
- 5ms Internal Soft-Start
- Fixed 400kHz Switching Frequency
- **PWM and Pulse Skip Modes**
- Peak Current Mode Control
- Internal Loop Compensation
- Over-Current Protection for Both MOSFETs
- Output Over-Voltage Protection
- Adjustable Under-Voltage Lockout
- Thermal Shutdown with Auto Recovery
- -40°C to +125°C Operating Temperature Range
- Available in a Green TSOT-23-6 Package

APPLICATIONS

Digital Television Printers

12V Distributed Power Supply Buses Industrial and Consumer Applications White Goods Audio Equipment Set Top Boxes

TYPICAL APPLICATION

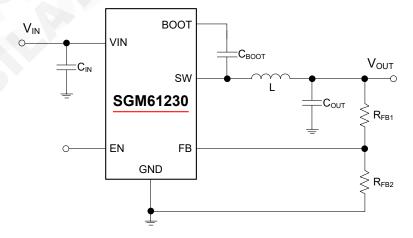
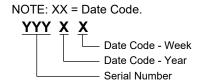


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION	
SGM61230	TSOT-23-6	-40°C to +125°C	SGM61230XTN6G/TR	CE9XX	Tape and Reel, 3000	

MARKING INFORMATION



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range	0.3V to 30V
EN and BOOT-SW Voltages	0.3V to 6V
SW Voltage	0.3V to 30V
SW (20ns transient) Voltage	5V to 30V
FB Voltage	0.3V to 3.5V
Package Thermal Resistance	
TSOT-23-6, θ _{JA}	50°C/W
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range	4.5V to 28V
EN and BOOT-SW Voltages	0.1V to 5.5V
SW Voltage	0.1V to 28V
FB Voltage	0.1V to 3V
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

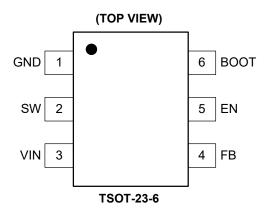
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE (1)	DESCRIPTION
1	GND	_	Device Ground Reference Pin.
2	SW	0	Switching Node: Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.
3	VIN	-	Input Supply Voltage Pin. VIN powers the internal control circuitry and the power converter. Decouple this pin for very high frequency and high di/dt transitions, with small and high frequency ceramic capacitors placed as close as possible between VIN and GND pins. VIN under-voltage is protected by a UVLO comparator.
4	FB	1	Feedback (Sense) Pin for Output Voltage and Programming. It is normally regulated at 0.6V. Tap the output feedback resistor divider to this pin.
5	EN		Device Enable Pin. Device will operate if EN voltage is high and will shut down if it is low. Device will be enabled if this pin is left float. EN pin can be used to increase the UVLO thresholds.
6	воот	0	Bootstrap Pin. Place a $0.1\mu F$ capacitor (C_{BOOT}) between BOOT and SW pins close to the device to provide the required drive voltage for the high-side switch. Do not place any series resistor with C_{BOOT} .

NOTE 1. O = Output; I = Input.

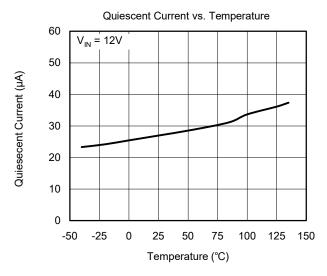
ELECTRICAL CHARACTERISTICS

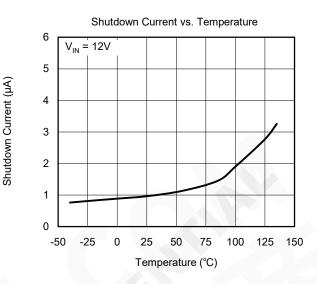
 $(T_J = +25^{\circ}C, V_{IN} = 4.5V \text{ to } 28V, \text{ unless otherwise noted.})$

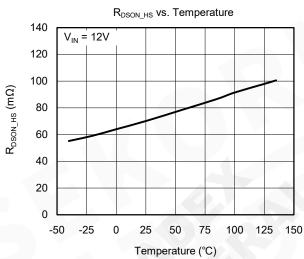
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply	•					
Input Voltage Range	V _{IN}		4.5		28	V
Non-Switching Quiescent Current	ΙQ	V _{EN} = 5V, V _{FB} = 1V		30		μΑ
Shutdown Current	I _{SD}	EN = GND		3		μΑ
Under-Voltage Lockout Threshold		Rising V _{IN}		4.1		V
Orider-voltage Lockout Trileshold	V_{UVLO}	Falling V _{IN}		3.75		V
Under-Voltage Lockout Hysteresis	V _{UVLO_HYS}			350		mV
Enable (EN Pin)						
Enable Threshold	V _{IH}	Rising		1.19		V
Enable Threshold	V _{IL}	Falling		1.09		V
Immust Cummant	I _{IL}	V _{EN} = 1V		0.4		μΑ
Input Current	I _{IH}	V _{EN} = 1.5V		1.5		μΑ
Feedback and Error Amplifier						
Feedback Voltage	V_{FB}	V _{IN} = 12V		0.6		V
Power Stage						
High-side FET On-Resistance	R _{DSON_HS}	$T_J = +25^{\circ}C$, $V_{BOOT} - V_{SW} = 5V$		70		mΩ
Low-side FET On-Resistance R _{DSON_LS}		$T_J = +25^{\circ}C, V_{IN} = 12V$		39		mΩ
Current Limit						
High-side Current Limit	I _{LIM_HS}	Maximum inductor peak current		5.4		Α
Low-side Current Limit I _{LIM_LS}		Maximum inductor valley current		4		Α
Oscillator						
Switching Frequency f _{SW}				400		kHz
Over-Temperature Protection						
Thermal Shutdown T _{SHDN}		Rising Temperature		165		℃
Thermal Shutdown Hysteresis T _{HYS}				10		°C
Timing Requirements			•	•	•	
Soft-Start Time	t _{ss}			5		ms

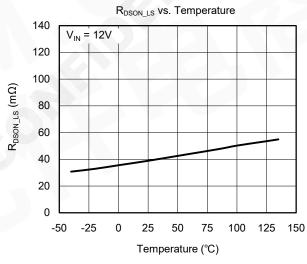
TYPICAL PERFORMANCE CHARACTERISTICS

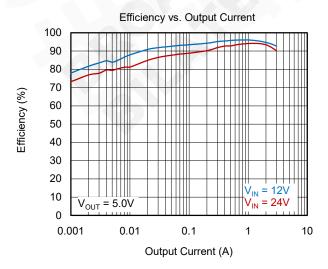
 T_J = +25°C, V_{IN} = 4.5V to 28V, unless otherwise noted.





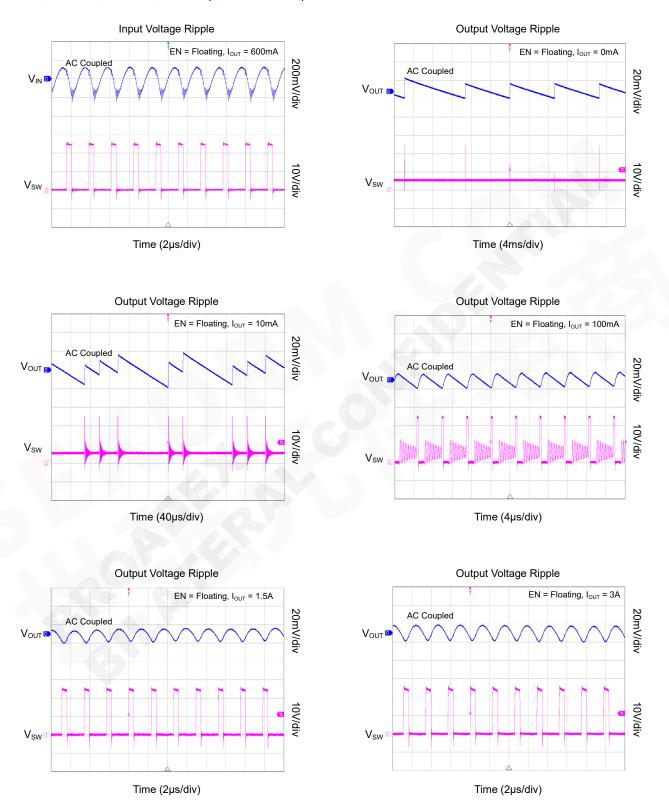






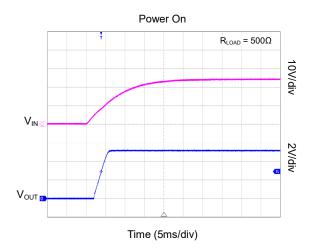
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 T_J = +25°C, V_{IN} = 24V, V_{OUT} = 5V, C_{IN} = 10 μ F, C_{OUT} = 2 × 22 μ F, unless otherwise noted.

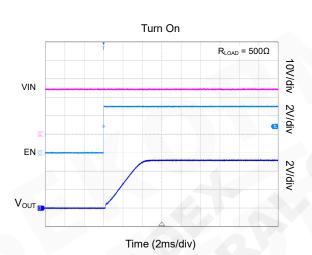


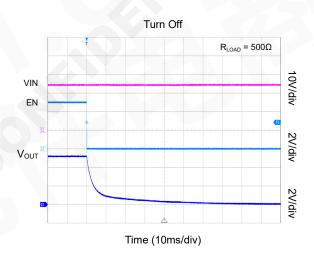
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

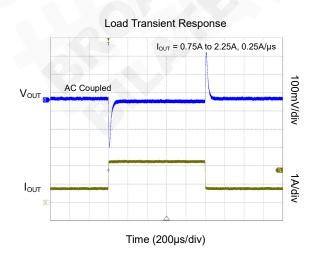
 T_J = +25°C, V_{IN} = 24V, V_{OUT} = 5V, C_{IN} = 10 μ F, C_{OUT} = 2 × 22 μ F, unless otherwise noted.











FUNCTIONAL BLOCK DIAGRAM

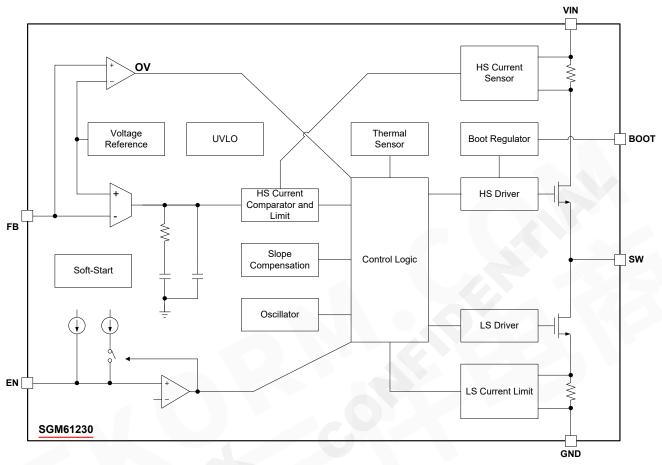


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The <u>SGM61230</u> is a 28V/3A synchronous step-down converter with over-current, short circuit and thermal protection. Two integrated low R_{DSON} N-MOSFETs (70m Ω high side and 39m Ω low side) allow continues operation at 3A output with high efficiency.

The device is powered up when V_{IN} exceeds the UVLO threshold (4.1V TYP). At no load and with no switching, the typical operating current is $30\mu\text{A}$ and when the device is disabled by EN pin, it is only $3\mu\text{A}$ (TYP). The internal loop compensation minimizes the BOM count and simplifies the design. The inrush current is also limited by an internal 5ms soft-start ramp.

Operating Principle

Peak current mode (PCM) control is used in the SGM61230 to regulate the output voltage. V_{OUT} is sensed by the external resistor divider on the FB pin and compared to the internal 0.6V voltage reference by a trans-conductance error amplifier. The error amplifier (EA) output (current) is fed to the internal compensation components between the EA output and GND to generate a voltage that is used as the peak current reference for comparing with the sensed high-side switch current. The output of this comparator (COMP) can reset the flipflop that controls the switches. This flipflop receives fixed frequency clock pulses from the internal 400kHz oscillator. In the normal operation the high-side switch is turned on in the beginning of each switching cycle. The current in the high-side switch starts to rise until the peak current reference is reached that resets the flipflop. This will turn off the high-side switch and turns on the low-side switch. The low-side switch stays on until the end of the cycle.

Slope Compensation

Peak current mode-controlled devices in general are subject to sub-harmonic oscillation instability at higher duty cycles (typically > 50%). To avoid this instability a compensating ramp signal is used. The ramp starts from zero in the beginning of each cycle with a specific slop and is added to the sensed high-side switch current before it is compared to the peak current reference.

Anti-High-Overload Mode

The <u>SGM61230</u> supports over load mode, when the output current continues over load while the system power up or in turbo mode, the <u>SGM61230</u> exports the maximize power and limit the maximum peak current in

high side and valley current in low side, the device keeps in cycle by cycle limit to obtain the system's power request. The SGM61230 does not shut down until the device heats and then goes to thermal shutdown. The load Increase, the output voltage goes low, if the output voltage drops to 20%, the device will go into short protection. It reduces current limit threshold and the switching frequency goes down due to reduce power dissipation and device goes into thermal shutdown. When the output current is low enough device goes into PFM mode.

Pulse Skip Mode (PSM) and PWM

In light load, OVP does not occur and the device can operate in the normal PWM, however to improve light load efficiency, the device is designed to skip some pulses by entering to the PSM mode. When the peak current is lower than 500mA typically, the device enters PSM. In PSM, when the output voltage is detected to be above the internal voltage reference level the error amplifier, the high-side MOSFET is kept off for a few cycles (skipping clock pulses) by clamping current reference until the output voltages are discharged below the internal voltage reference level. Note that the integrated current comparator operates based on the peak inductor current and the average load current may vary depending on the output filters and load type.

Enable Pin and UVLO Adjustment

The EN pin can be used to turn the device on and off or to change the UVLO thresholds. The device is enabled when the EN pin voltage exceeds its high threshold. A low EN voltage disables the device brings it to the low-quiescent (I_Q) state.

The EN pin is internally pulled up by a small current source (I_P) so the device is enabled if EN pin is floated. An open drain or open collector output can be used to control the EN pin.

 V_{IN} is monitored by the internal under-voltage lockout circuit and if it is below UVLO threshold, the device is disabled. The internal UVLO has a 350mV hysteresis. If higher thresholds are needed, EN pin can be used as shown in Figure 3.

The EN pull-up current is used to set the hysteresis. The pull-up current is increased by I_{lH} - I_{lL} when the EN pin exceeds its high threshold. Use Equations 1 and 2 to calculate the R_1 and R_2 values for the desired UVLO low (V_{UV_L}) and high $(V_{UV\ H})$ thresholds.

DETAILED DESCRIPTION (continued)

$$R_{1} = \frac{V_{UV_{-}L} \times V_{IH} - V_{UV_{-}H} \times V_{IL}}{V_{IL} \times I_{IH} - V_{IH} \times I_{IL}}$$
(1)

$$R_{2} = \frac{R_{2} \times V_{IL}}{V_{UV_{L}} - V_{IH} + R_{1} \times I_{IH}}$$
 (2)

where:

$$\begin{split} I_{IL} &= 0.4 \mu A \, (TYP) \\ I_{IH} &= 1.5 \mu A \, (TYP) \\ V_{IL} &= 1.09 V \, (TYP) \\ V_{IH} &= 1.19 V \, (TYP) \end{split}$$

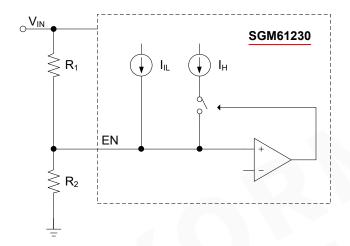


Figure 3. Adjustable VIN Under-Voltage Lockout

Output Voltage Programming

The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use resistors with 1% tolerance or better because it directly affects the output accuracy. Use Equation 3 and Figure 1 to calculate the output voltage. To improve efficiency at light load consider larger resistors. Start with $100 \text{k}\Omega$ for the upper resistor (R_{FB1}). Note that if $R_{\text{FB1}} ||R_{\text{FB1}}|$ is too high, the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{FB} \times \left[\frac{R_{FB1}}{R_{FB2}} + 1 \right]$$
 (3)

Internal Voltage Reference and Soft-Start

The <u>SGM61230</u> device has an internal 0.6V reference (V_{REF}) to program the output at the desired level. The output voltage is determined by the reference voltage seen by the error amplifier. When the converter starts (or is enabled), an internal ramp voltage begins to rise from near 0V to slightly above 0.6V with a ramp time of 5ms. The lower of V_{REF} and this ramp is used as

reference for the error amplifier, therefore during startup the ramp provides a soft-start for the output. The soft-start is needed to avoid high inrush currents caused by rapid increase of output voltage across output capacitors and the load. Without a soft-start the current limiting protections could trigger that interrupts the monotonic rising of the load voltage that may result in instability or improper system initialization.

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than V_{IN} is needed. Bootstrapping technique is used to provide this voltage from the switching node using a $0.1\mu\text{F}$ bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations.

Over-Current Protection (OCP)

The device is protected from over-current conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs.

High-side MOSFET Over-Current Protection

The internal peak current mode controller provides an inherent current limiting capability for the high-side switch on a cycle-by-cycle basis. When high-side switch current exceeds peak current limit threshold, high-side switch is turned off, until the next cycle.

Low-side MOSFET Over-Current Protection

The low-side MOSFET current is also monitored for over-current protection. Normally this MOSFET sources current to the load (source to drain direction) while the inductor current is decreasing. At the end of each cycle, this current is compared to the preset low-side current-limit (I_{LIM_LS}). If the inductor valley current exceeds the low-side current limit, the high-side MOSFET will not turn on in the next cycle and the low-side MOSFET continues to conduct (cycle skipped). The high-side switch turns on again when the valley current falls below I_{LIM_LS} at the start of another cycle (Figure 4).

During an over-current fault, the above limits cause cycle skipping that slowdowns the switching frequency and reduces the output voltage (due to reduced duty cycle).

DETAILED DESCRIPTION (continued)

Output Short Circuit Protection

When the output voltage down to 20% of set value, the device goes into short circuit mode, a fold-back mode will limit the current output. The high-side peak current limit to 2.4A (TYP) and the valley current limit to 1.4A (TYP), then it avoids the device thermal shutdown by the power dissipation.

A short circuit is detected when V_{FB} falls below 0.12V (TYP). In this condition the current limits of both switches are internally reduced to less than half of the normal value (fold back). This will reduce the constant output current during an output short and prevents overheating. During the soft-start period there is no foldback and the current limits are normal.

Output Over-Voltage Protection (OVP)

An over-voltage protection is included in the device to minimize the output voltage overshoots that may occur after recovery from an output fault or a large unloading transient. The FB pin voltage is compared with the OVP thresholds. If the V_{FB} exceeds 108% of the V_{REF} , the high-side switch is forced to turn off. When the V_{FB} falls below 104%, the high-side switch is again allowed to turn on.

Thermal Shutdown

If the junction temperature exceeds $+165^{\circ}$ C (TYP) the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

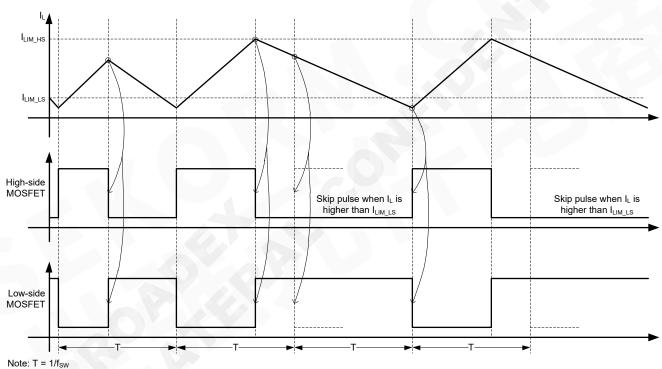


Figure 4. Over-Current Protection for MOSFETs

APPLICATION INFORMATION

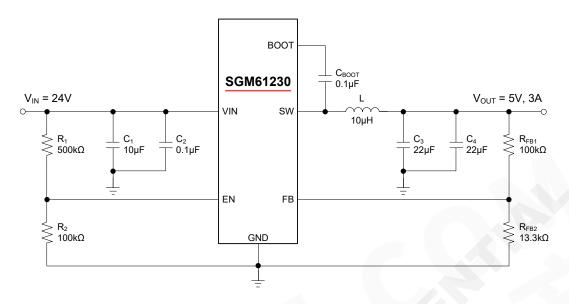


Figure 5. A Reference Design for 5V, 3A Application

Application Notes

- 1. A 10pF feedforward capacitor is optioned to improve the response.
- 2. When the output is shorted, a large input capacitor is required to ensure that the output voltage ripple is lower than 1V, otherwise the device may not be stable.
- 3. To reduce the output ripple and keep the device stable, the output capacitor must be large. The recommended value should not be lower than $22\mu\text{F} + 22\mu\text{F}$, and a $100\mu\text{F}$ output capacitor will be very helpful for reducing ripple.
- 4. 0.1% R_{FB1}, R_{FB2} will be chosen to improve the output voltage precision, if it is needed.

Layout Guide

Layout guide schematic for PCB Layout.

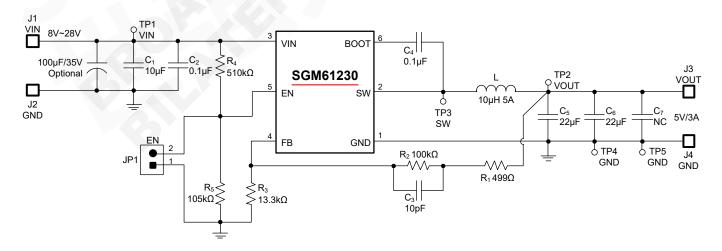
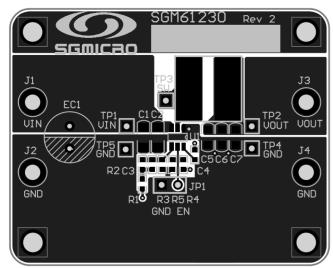


Figure 6 Schematic for PCB Layout

APPLICATION INFORMATION (continued)





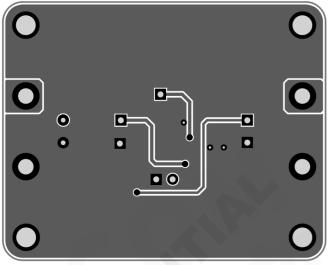
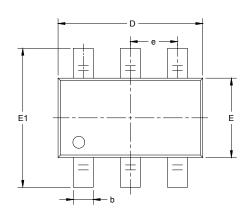
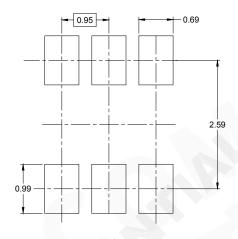


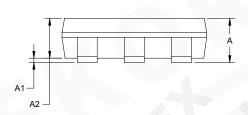
Figure 8 PCB Bottom Layer

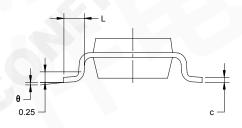
PACKAGE OUTLINE DIMENSIONS TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)

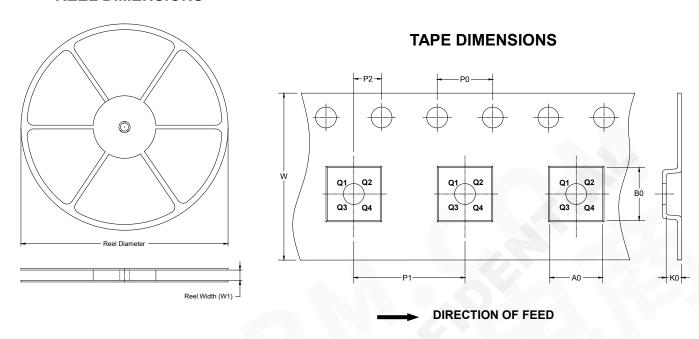




Symbol		nsions meters	Dimensions In Inches		
	MIN	MAX	MIN	MAX	
Α		1.000		0.043	
A1	0.000	0.100	0.000	0.004	
A2	0.700	0.900	0.028	0.039	
b	0.300	0.500	0.012	0.020	
С	0.080	0.200	0.003	0.008	
D	2.850	2.950	0.112	0.116	
E	1.550	1.650	0.061	0.065	
E1	2.650	2.950	0.104	0.116	
е	0.950	BSC	0.037	BSC	
L	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	

TAPE AND REEL INFORMATION

REEL DIMENSIONS

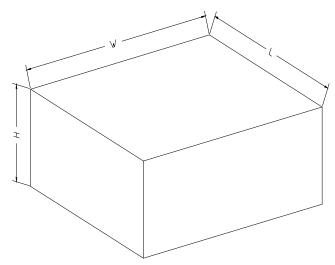


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-6	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton	
7" (Option)	368	227	224	8	
7"	442	410	224	18	200007