SGM6609
High Current Synchronous Step-Up Converter with Adjustable Current Limit

GENERAL DESCRIPTION

The SGM6609 is a high current, synchronous step-up converter with programmable low-side MOSFET peak current limit of 500mA to 3.5A. It is ideal for preventing input current from overloading system power in PCI-E card applications based on WCDMA/Edge/GPRS/ TD-SCDMA, PCI-E card GSM high load pulse applications. With a suitable ultra-cap or super-cap, the SGM6609 ensures that output voltage meets load power requirements when large load pulses are applied. It is also ideal for CDMA/Evdo-A/Evdo-B and other industry modem continuous load current applications.

The output voltage of the SGM6609 is programmed from 3.0V to 5.0V by an external resistive divider. Optimized internal compensation provides fast transient response with no external components. Light load switching frequency modulation and low quiescent current maintains high efficiency performance for light load mode conditions.

The low-side power MOSFET peak current limit of 500mA to 3.5A is set via an external resistor to protect the system power from overload.

Reverse blocking is integrated to prevent current from flowing back to the input. The SGM6609's true load disconnect function isolates the output from the input when the device is disabled. Output over-voltage, short-circuit, and over-temperature protection are also integrated to protect the SGM6609 from these fault conditions.

The SGM6609 is available in Green TDFN-3×3-12L package and is rated over the -40℃ to +85℃ temperature range.

FEATURES

- **2.4V to 5.0V Input Voltage Range**
- **Adjustable 3.0V to 5.0V Output Voltage**
- **Programmable NMOS Peak Current Limit: 500mA to 3.5A**
- **Synchronous Boost Rectification and Internal Compensation**
- **1.2MHz Switching Frequency**
- **Reverse Current Blocking**
- **True Load Disconnect in Shutdown**
- **Up to 95%Efficiency**
- **Power-Good Indication**
- **Programmable Over-Voltage Protection**
- **Over-Temperature and Short-Circuit Protection**
- **Available in Green TDFN-3×3-12L Package**
- **-40℃ to +85℃ Operating Temperature Range**

APPLICATIONS

PC Cards (PCMCIA) Modems
PCI-E Modem Cards
WCDMA/Edge/GPRS/TD-SCDMA
CDMA/Evdo-A/Evdo-B
Industry Modems
USB Modems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	MARKING INFORMATION	PACKING OPTION
SGM6609	TDFN-3×3-12L	-40℃ to +85℃	SGM6609YTDF12G/TR	SGM 6609DF XXXXX	Tape and Reel, 4000

NOTE: **XXXXX** = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage Range ..... -0.3V to 6V
Supply Voltage on SW, VOUT, EN, FB, $\overline{PG}$ ..... -0.3V to 6V
PGND to AGND ..... -0.3V to 0.3V
Package Thermal Resistance
TDFN-3×3-12L, θ_{JA} ..... 52.1℃/W
Junction Temperature ..... 150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... 260℃
ESD Susceptibility
HBM 4000V
MM 200V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.4V to 5.0V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

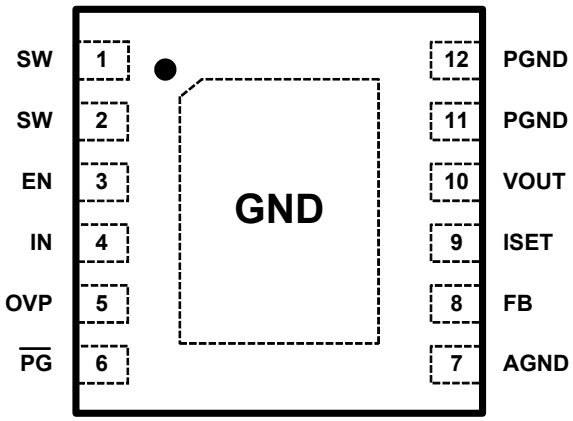
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×3-12L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	SW	Switching Node Tied to Drain of Internal N-Channel MOSFET and Source of Internal P-Channel MOSFET. Connect this pin to the external power inductor.
3	EN	Input Enable Pin. Logic high to enable the boost. Logic low to disable the IC.
4	IN	Input Voltage. Supplies the IC at startup.
5	OVP	Over-Voltage Protection Pin. This pin is connected to an external resistor divider to set the over voltage threshold. To disable the over voltage feature, short this pin to ground.
6	$\overline{PG}$	Power-Good Signal (Active Low). $\overline{PG}$ is an open-drain, active-low output. $\overline{PG}$ is pulled low when the feedback voltage exceeds 95% of the target voltage.
7	AGND	Non-Power Signal Ground Pin.
8	FB	Feedback Input Pin. This pin is connected to an external resistor divider which programs the output voltage with feedback voltage of 0.6V.
9	ISET	Peak Current Limit Programmable Input. An external resistor from ISET to ground is adopted to program the low-side MOSFET peak current limit between 500mA and 3.5A.
10	VOUT	Boost Converter Output Voltage. This pin is connected to the P-Channel synchronous MOSFET source. Bypass with ceramic capacitor to GND.
11, 12	PGND	Power Ground. PGND is internally connected to the source of the low-side N-Channel MOSFET.
Exposed Pad	GND	Power Ground Exposed Pad. Must be connected to ground plane.

ELECTRICAL CHARACTERISTICS

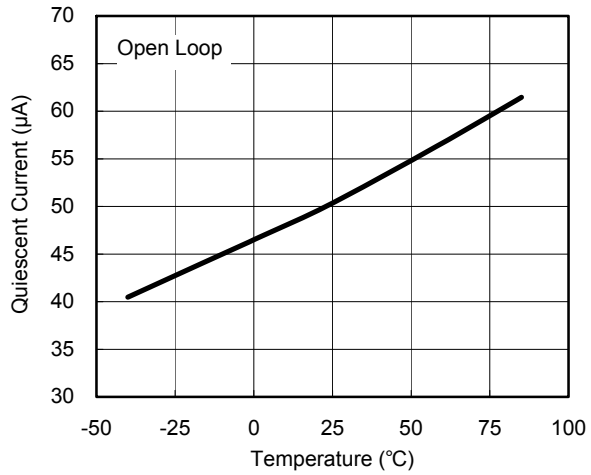
(V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.4		5.0	V
Minimum Start-Up Voltage	$V_{IN(MIN)}$			2.3		V
Output Voltage Range	V_{OUT}		3.0		5.0	V
Input Under-Voltage Lockout	V_{UVLO}	V_{IN} Rising, Hysteresis = 0.2V	2.15	2.25	2.35	V
Quiescent Supply Current	I_Q	No-Load Current; Not Switching		50	70	μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = GND, V_{IN} = 5.0V			1	μA
Feedback Accuracy	V_{FB}	T_A = +25℃, V_{FB} = 600mV	-2		+2	%
		T_A = -40℃ to +85℃, V_{FB} = 600mV	-3		+3	
Feedback Leakage Current	I_{FB}	V_{FB} = 0 to 1.0V	-1		+1	μA
Load Regulation	$\Delta V_{OUT}/I_{OUT}$	V_{IN} = 3.3V, V_{OUT} = 3.8V, 0 to 2.5A Load		1		%/A
Line Regulation	$\Delta V_{OUT}/V_{IN}$	V_{IN} = 2.4V to V_{OUT}, I_{OUT} = 10mA		0.3		%/V
Output Over-Voltage Protection Threshold	V_{OVP}		0.55	0.60	0.65	V
Switching Frequency	f_{SW}			1.2		MHz
Maximum Duty Cycle	D			90		%
Minimum On-Time	$t_{ON(MIN)}$			80		ns
High-side P-Channel On-Resistance	$R_{ON(PMOS)}$			140		mΩ
Low-side N-Channel On-Resistance	$R_{ON(NMOS)}$			80		mΩ
Low-side Peak Current Limit Threshold	I_{LIMPK}	T_A = +25℃, R_{SET} = 60.4kΩ	1.9	2.55	3.2	A
ENABLE, POWER-GOOD AND START-UP FEATURES						
Logic Input Threshold High for EN	V_{IH}		1.5			V
Logic Input Threshold Low for EN	V_{IL}				0.4	V
EN Input Low Current	I_{EN}	V_{EN} = GND or 5.0V	-1	0.01	4	μA
Power-Good Threshold		FB Rising, Hysteresis = 10%		95		%
$\overline{PG}$ On-Resistance	$R_{\overline{PG}}$	V_{FB} = 0.62V, I_{SINK} = 10μA		450		Ω
THERMAL						
Over-Temperature Shutdown Threshold	T_{SD}	Temperature Rising		150		℃
Over-Temperature Shutdown Hysteresis	T_{HYS}			20		℃

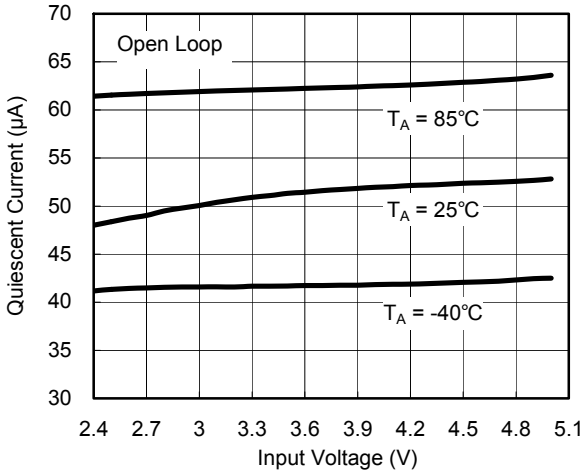
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND, T_A = +25℃, unless otherwise noted.

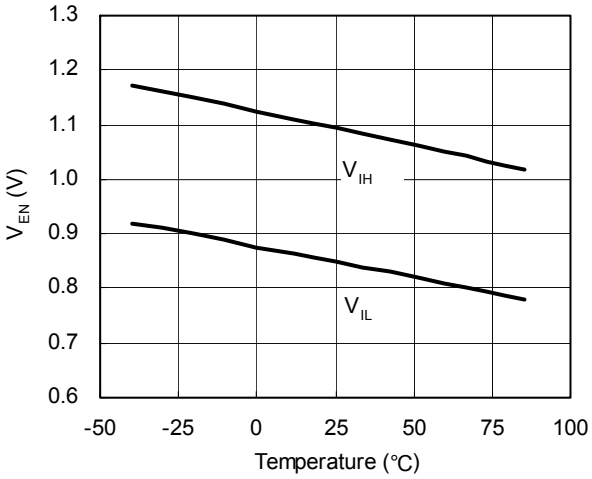
Quiescent Current vs. Temperature



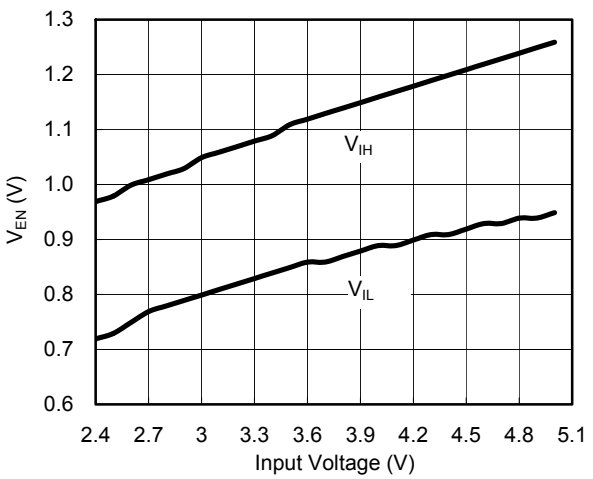
Quiescent Current vs. Input Voltage



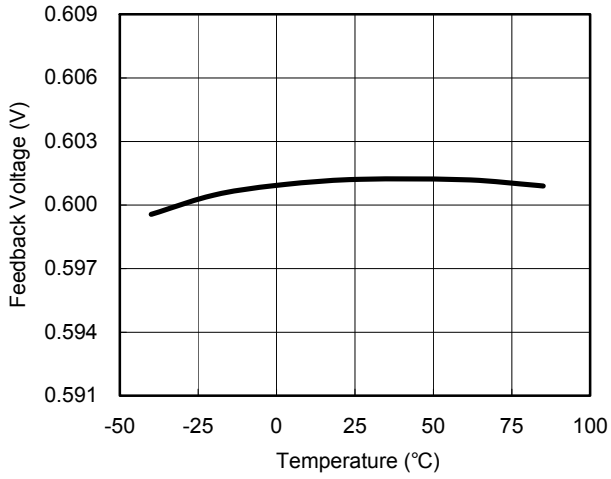
Enable Threshold vs. Temperature



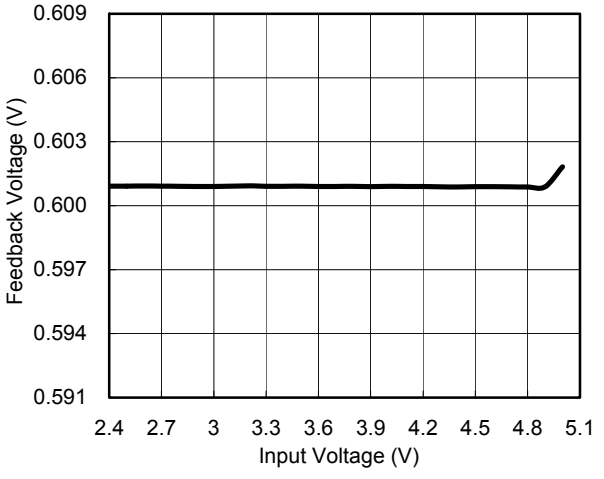
Enable Threshold vs. Input Voltage



Feedback Voltage vs. Temperature



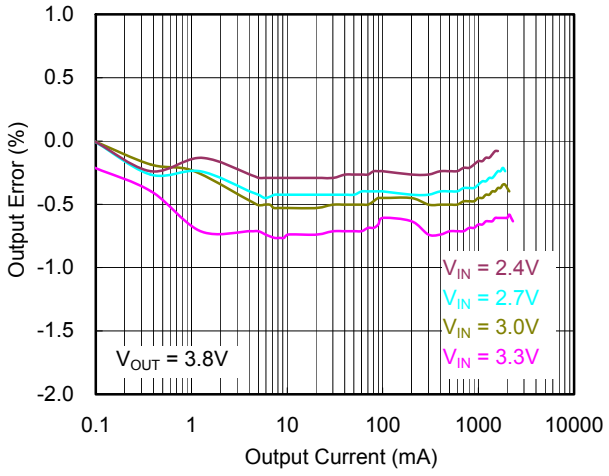
Feedback Voltage vs. Input Voltage



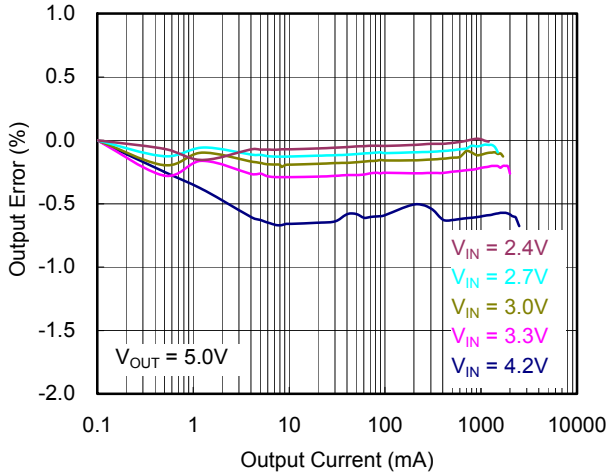
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND, T_A = +25℃, unless otherwise noted.

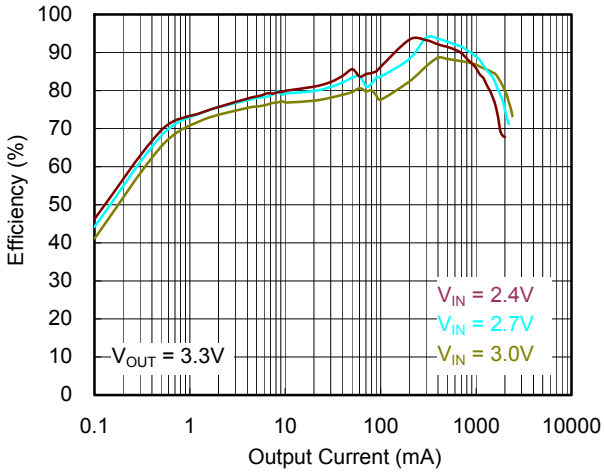
Load Regulation



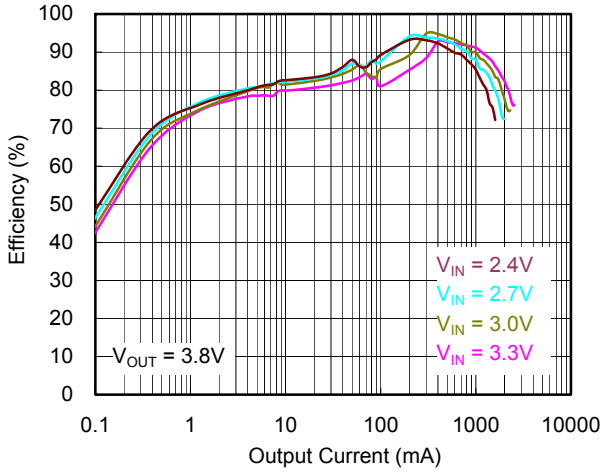
Load Regulation



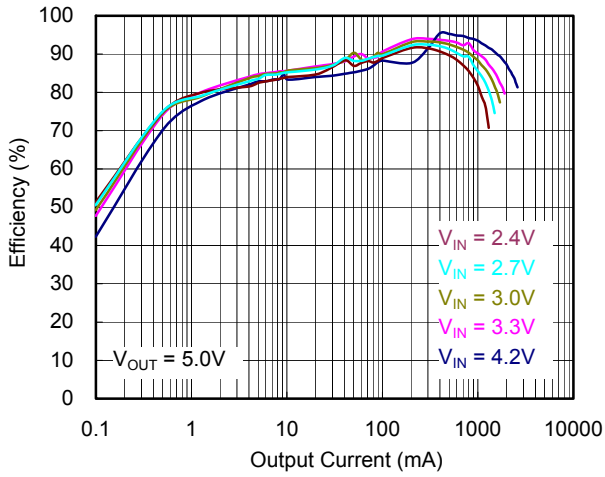
Efficiency vs. Output Current



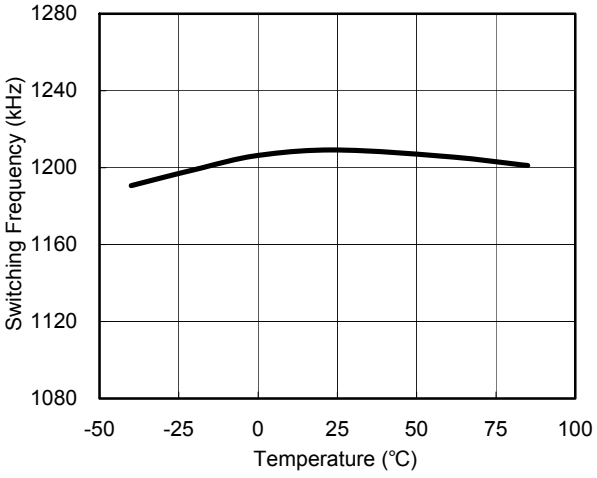
Efficiency vs. Output Current



Efficiency vs. Output Current



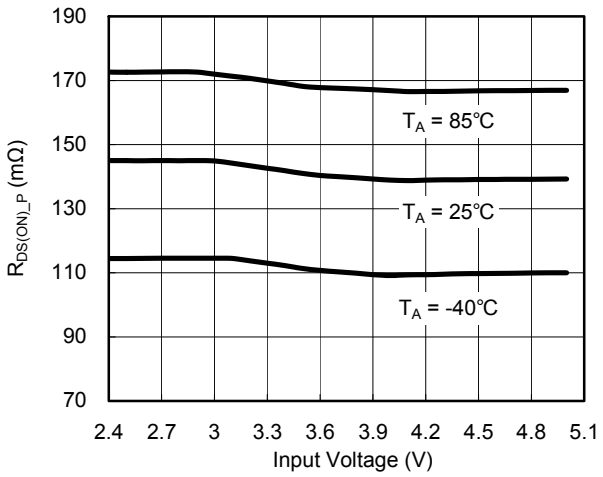
Switching Frequency vs. Temperature



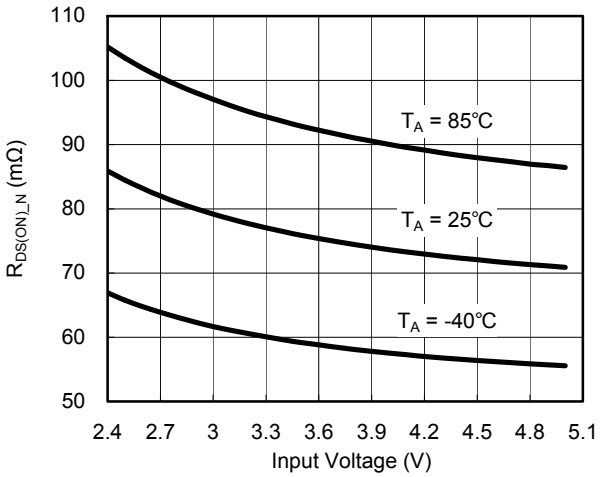
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND, T_A = +25℃, unless otherwise noted.

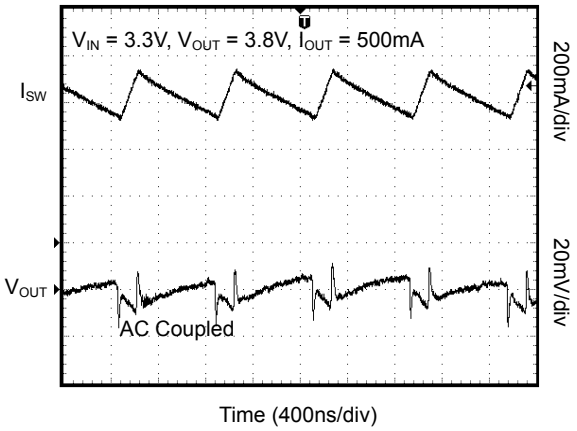
$R_{DS(ON)\_P}$ vs. Input Voltage



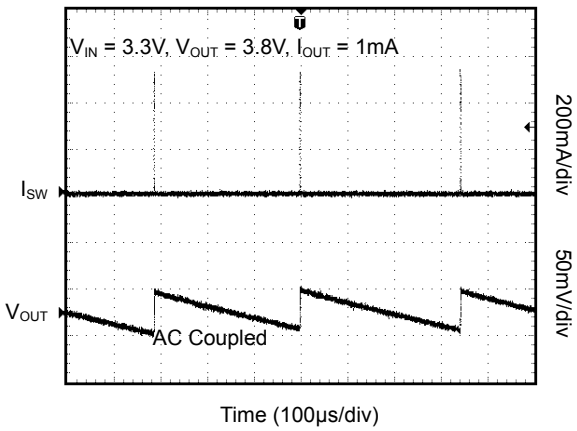
$R_{DS(ON)\_N}$ vs. Input Voltage



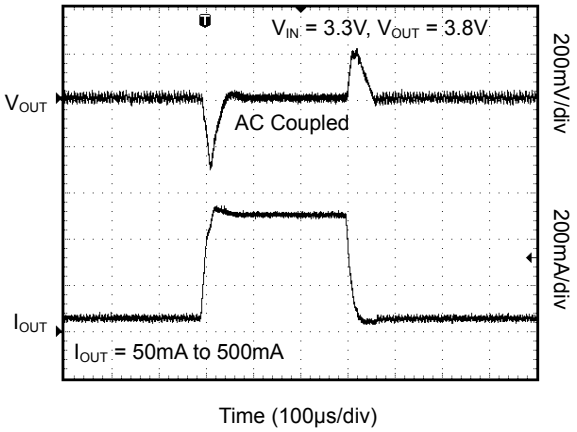
Output Ripple



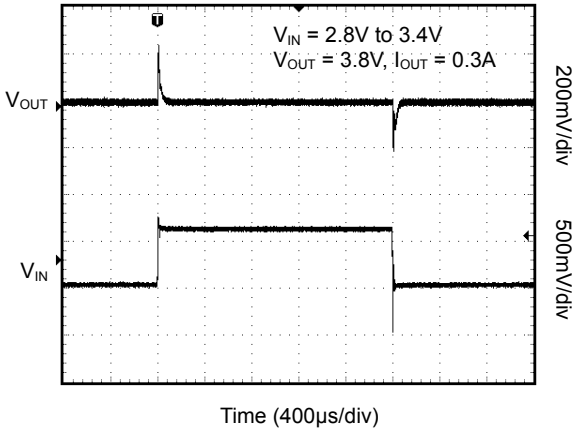
Output Ripple



Load Transient Response



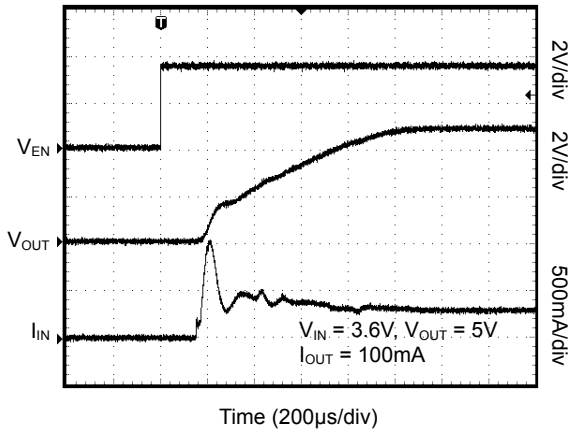
Line Transient Response



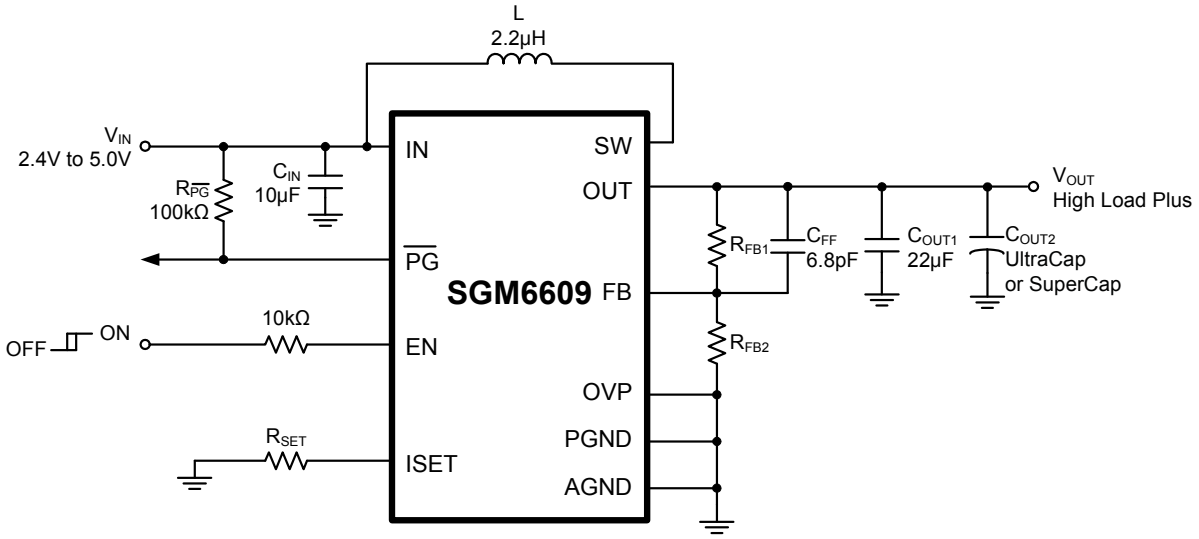
TYPICAL PERFORMANCE CHARACTERISTICS

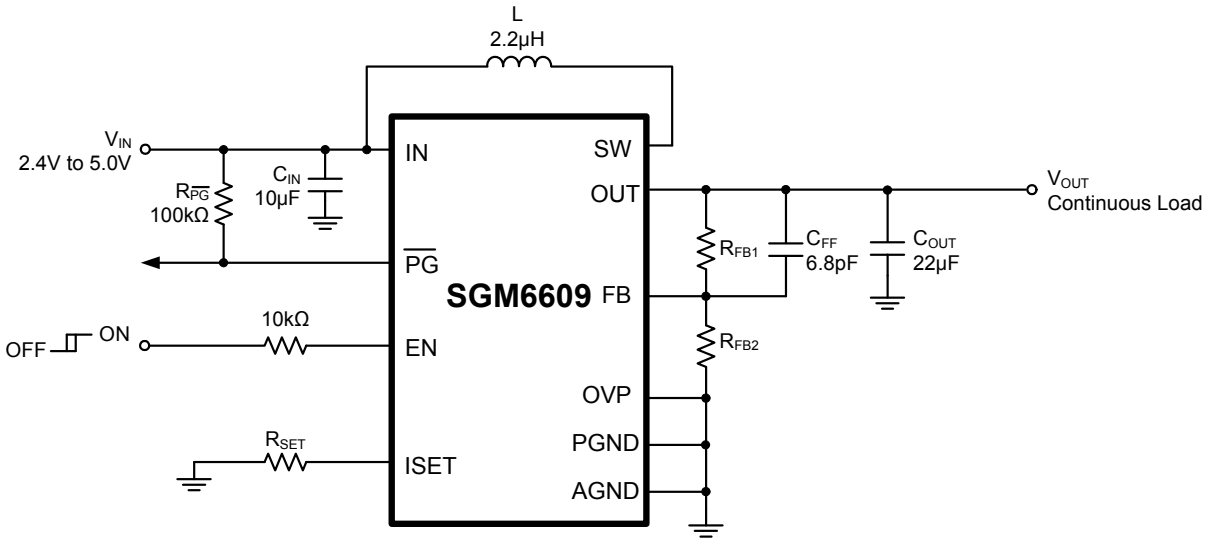
V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND, T_A = +25℃, unless otherwise noted.

Soft Start

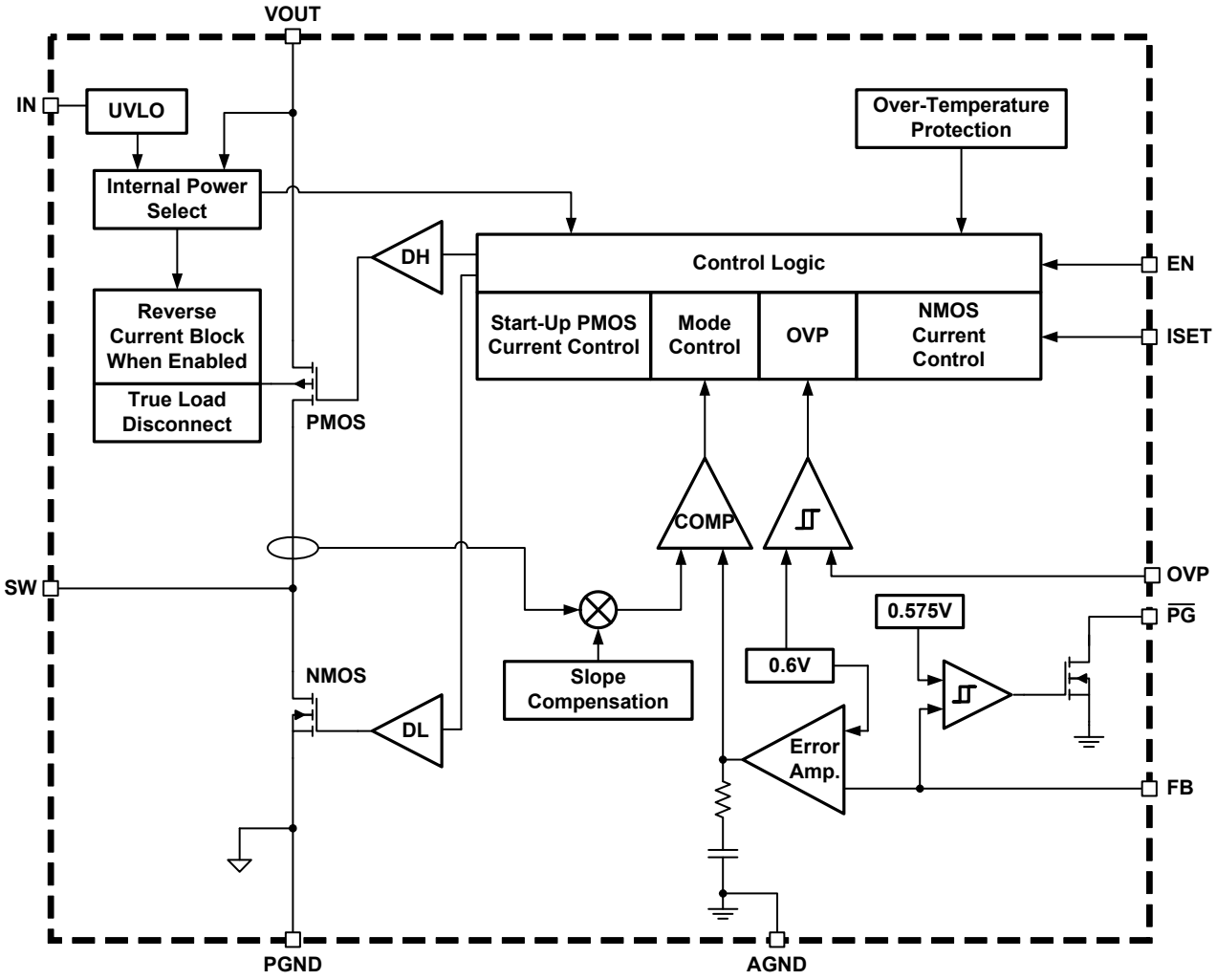


TYPICAL APPLICATIONS





FUNCTIONAL BLOCK DIAGRAM



OPERATION

The SGM6609 synchronous step-up converter is targeted for PC card GSM/GPRS/3G and WiMax modem card applications. It includes a current limit to ensure fast, controlled startup and continuous operation with the PCMCIA specifications.

The high 1.2MHz switching frequency of the SGM6609 facilitates output filter component size reduction for improved power density and reduced overall footprint. It also provides greater bandwidth and improved transient response over other lower frequency step-up converters. The compensation is integrated with three external components C_{IN}, C_{OUT} and L. Low $R_{DS(ON)}$ synchronous power switches provide high efficiency for heavy load conditions. Switching frequency modulation and low quiescent current maintains high efficiency for light load mode conditions. In addition to the improved efficiency, the synchronous step-up has the added performance advantage of true load disconnect during shutdown (<1μA shutdown current), reverse current blocking when enabled, and short-circuit protection.

PWM Control Scheme for Light Load

The SGM6609 is a fixed frequency PWM peak current mode control step-up converter. For light load condition, the converter stays in a variable frequency (light load) mode to reduce the dominant switching losses. In addition to light load operation, a zero current comparator blocks reverse current in the synchronous P-Channel MOSFET, forcing DCM operation at light load. These controls, along with very low quiescent current, help to maintain high efficiency over the complete load range without increased output voltage ripple during light load conditions.

Shutdown and True Load Disconnect

A typical synchronous step-up (boost) converter has a conduction path from the input to the output via the parasitic body diode of the P-Channel MOSFET when the converter shuts down. The SGM6609 design uses a special power selection for the substrate to keep the parasitic body diode in off-state during shutdown and startup. This enables the SGM6609 to provide true load disconnect during shutdown.

When EN is set to logic low, the step-up converter is forced into shutdown state with less than 1μA input current.

Start-Up

When initially powering up, the load disconnect feature allows the output voltage to be less than the input voltage. In order to avoid large surge current when the regulator is enabled, the SGM6609 operates a soft-start mode to softly charge the large output capacitor.

Programmable NMOS Peak Current Limit

The current limit of the internal low-side NMOS power switch is programmable by an external resistor. During the inductor charge cycle, the current through the NMOS device is sensed. When this current reaches the value set by the R_{SET} resistor, the low-side NMOS switch is turned off. The NMOS current limit is an instantaneous peak current measurement and should be set high enough to allow the desired average current. The application section discusses proper selection of R_{SET} resistor values.

Power-Good Indication

To indicate output voltage OK, an open-drain output $\overline{PG}$ pin is designed to pull down when the output voltage increases to 95% of the nominal voltage level. The pin will be pulled up when the output voltage drops below 85% of the nominal output level.

Over-Voltage Protection

The SGM6609's over-voltage protection function prevents the output voltage from exceeding the programmed over-voltage point via an external resistor divider when output voltage has the possible risk of over-shoot. Resistors R_1 and R_2 in Figure 1 program the over-voltage trip point. 100kΩ is a good resistance for R_2 with good noise immunity and reduced no load input current. Calculate the value of R_1 using the following formula:

$$R_1 = \frac{R_2 \times V_{OUT\_OVP}}{0.6} - R_2$$

As an example, for a 5.5V OVP setting, R_1 is 820kΩ when R_2 is 100kΩ. If the over-voltage protection function is not used, connect the OVP pin to ground.

OPERATION

Over-Temperature Protection

An over-temperature event occurs when the SGM6609's junction temperature exceeds the over-temperature protection threshold. In the case, the SGM6609's over-temperature protection circuitry completely disables switching and the PMOS current limit serves to control the current level to avoid damage to the step-up converter. When the over-temperature fault condition is removed, the boost recovers regulation automatically.

Short-Circuit Protection

When a short-circuit fault occurs, the internal overload control circuit will effectively limits the output current under such fault conditions. When the fault is removed, SGM6609 recovers to normal operation automatically.

APPLICATION INFORMATION

R_{SET} Selection for Programmable Current Limit

The current limit of the internal low-side NMOS power switch is programmable by an external resistor connected from ISET to ground.

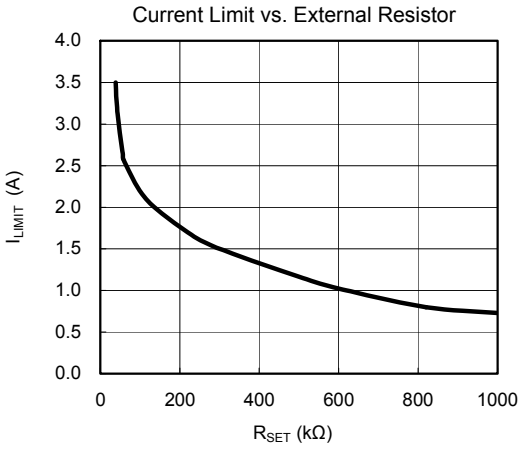


Table 1 gives standard 1% standard metal film resistor example values for NMOS current limit programming.

Table 1. Examples of 1% Standard Resistor Value of R_{SET}

R_{SET} (kΩ)	I_{LIMIT} (A)
1000	0.73
820	0.8
620	1
510	1.15
300	1.5
220	1.7
115	2.1
60.4	2.55
56	2.65
43	3.15
39	3.5

Output Voltage Programming

The output voltage of the SGM6609 may be programmed from 3.0V to 5.0V with an external resistive voltage divider. Resistors R_{FB1} and R_{FB2} in Figure 1 program the output voltage as shown by the following equation:

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \times R_{FB2}$$

where V_{FB} is the 0.6V feedback reference voltage.

To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the suggested value for R_{FB2} is 100kΩ. Table 2 summarizes the resistor values with R_{FB2} set to 100kΩ for good noise immunity and 6μA increased load current and gives some 1% standard metal film resistor values for R_{FB1} at different output voltage settings.

Table 2. 1% Standard Resistor Examples for Different Output Voltages

V_{OUT} (V)	R_{FB2} = 100kΩ R_{FB1} = (kΩ)
3	402
3.3	453
3.6	499
3.8	536
4.2	604
4.5	649
5	732

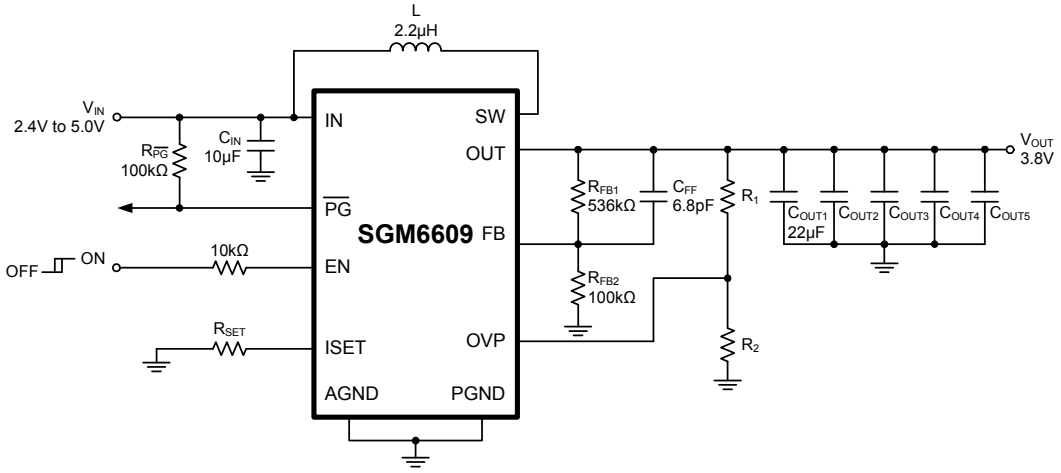


Figure 1. SGM6609 Evaluation Board Schematic

APPLICATION INFORMATION

Inductor Selection

The SGM6609 is designed to operate with a 2.2μH inductor for all input/output voltage combinations. For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

Input Capacitor

Select a low ESR ceramic capacitor with a value of at least 10μF as the input capacitor. The input capacitor should be placed as close to the IN and PGND pins as possible in order to minimize the stray resistance from the converter to the input power source.

Output Capacitor

The output capacitor provides energy to the load when the high-side MOSFET is switched off. The output capacitance together with the boost switching frequency, duty cycle, and load current value determine the capacitive output voltage ripple when the boost operation is in the continuous PWM state.

$$\Delta V_{OUT} = \frac{I_{OUT} \times D}{C_{OUT} \times f_{SW}}$$

where D is the duty ratio of low-side MOSFET turn-on time divided by the switching period. It is calculated using the equation:

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

The output capacitor's ESR increases the output ripple by I_{OUT} × ESR. The total output ripple is:

$$\Delta V_{OUT} = I_{OUT} \times ESR + \frac{I_{OUT} \times D}{C_{OUT} \times f_{SW}}$$

So the minimum recommended output capacitor value may be determined by:

$$C_{OUT} \geq \frac{I_{OUT} \times D}{\Delta V_{OUT} - I_{OUT} \times ESR} \times \frac{1}{f_{SW}}$$

High Load Pulse Application

Together with a large value output capacitor or super-cap, the SGM6609 can support a higher load pulse in lower input current limited applications such as GSM burst mode in WCDMA, Edge, GPRS and TD-SCDMA applications. The large capacitance is determined by NMOS peak current limit, inductor current ripple, V_{IN}, V_{OUT}, load pulse high current level and elapsed time. The capacitor value can be calculated using the following three steps as follows:

First calculate the SGM6609's load current from the expected I_{LIM} based on an approximation of input current equaling I_{LIM} because the inductor current ripple is low enough when compared to the input current:

$$I_{OUT\_BOOST} = \frac{V_{IN} \times I_{LIM} \times \eta}{V_{OUT}}$$

Second, calculate the maximum current the large capacitor C_{OUT} should provide:

$$I_{COUT} = I_{LOAD\_PEAK} - I_{OUT\_BOOST}$$

Finally, derive the C_{OUT} at a certain load-on period t_{ON}:

$$C_{OUT} = \frac{I_{OUT} \times t_{ON}}{\Delta V_{OUT}}$$

To consider a real capacitor may have 20% tolerance, the selected capacitance should be 20% higher than the calculated value. Example: A 2.0A, 217Hz 12.5% duty cycle load pulse is applied on 3.8V V_{OUT} at 3.3V V_{IN}. An input peak current limit of 2.4A and a V_{OUT} drop of less than 400mV are required. Under these conditions, with 90% efficiency, the SGM6609's output current is:

$$I_{OUT\_BOOST} = \frac{3.3 \times 2.4 \times 90\%}{3.8} = 1.876A$$

The maximum current necessary for the large capacitor value is:

$$I_{COUT} = 2.0 - 1.876 = 0.124A$$

t_{ON} is 593μs for a 217Hz 12.5% duty cycle load pulse. Considering a 20% capacitance tolerance, the minimum capacitance should be 220μF.

APPLICATION INFORMATION

Layout Guidance

For best performance of the SGM6609, the following guidelines should be followed when designing the PCB layout:

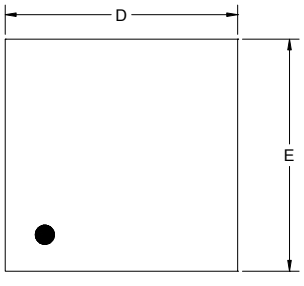
1. Make the power trace as short and wide as possible, including the input/output power lines and switching node, etc.

2. Connect the analog and power grounds together with a single short line and connect all low current loop grounds to analog ground to decrease the power ground noise on the analog ground and achieve better load regulation.

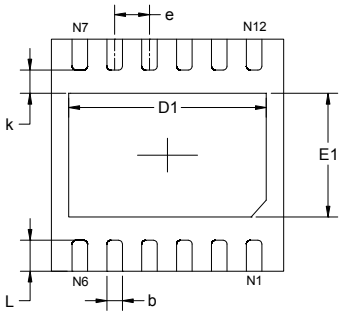
3. For good power dissipation, connect the exposed pad under the package to the top and bottom ground planes by PCB pads.

PACKAGE OUTLINE DIMENSIONS

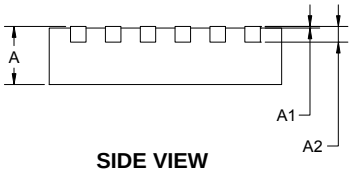
TDFN-3×3-12L



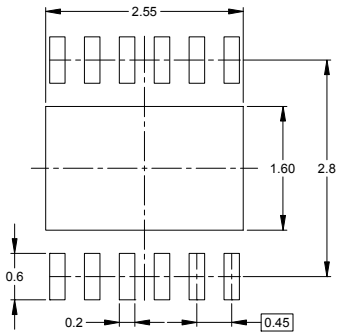
TOP VIEW



BOTTOM VIEW



SIDE VIEW

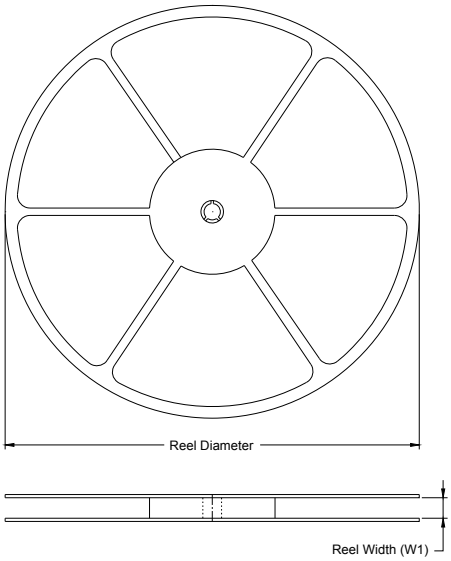


RECOMMENDED LAND PATTERN (Unit: mm)

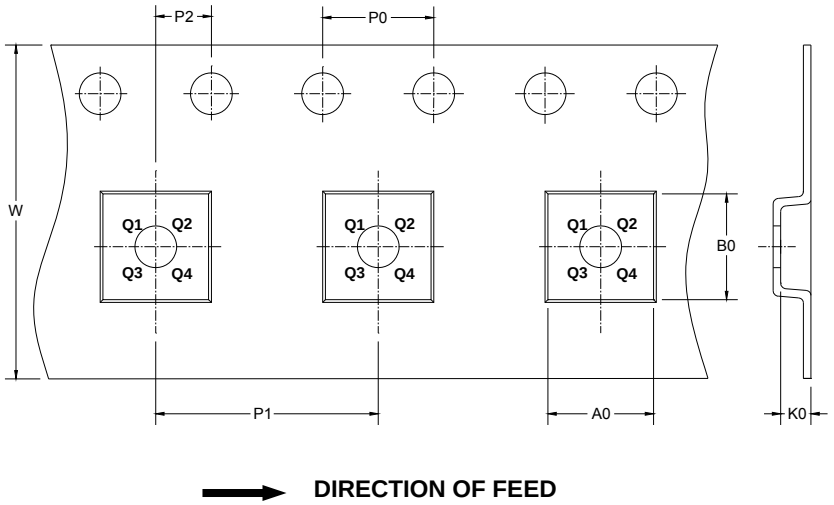
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.924	3.076	0.115	0.121
D1	2.450	2.650	0.096	0.104
E	2.924	3.076	0.115	0.121
E1	1.500	1.700	0.059	0.067
k	0.200 MIN		0.008 MIN	
b	0.150	0.250	0.006	0.010
e	0.450 TYP		0.018 TYP	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



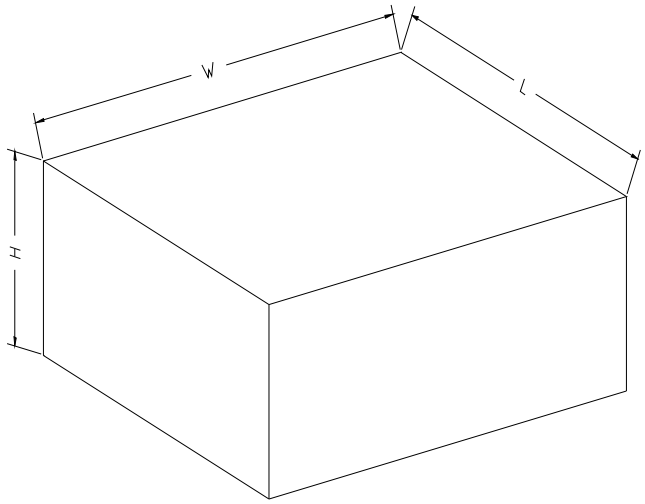
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-12L	13″	12.4	3.3	3.3	1.1	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002