SGM6606
5.0V/2.5A Output Synchronous Step-Up Converter with Programmable Current Limit for Output or Input

GENERAL DESCRIPTION

The SGM6606 is a high current, synchronous step-up regulator with a programmable input or output current limit. It is ideal to prevent the output current of SGM6606 from overloading or it limits the input current from battery or power source in standard interface, such as PCMCIA, PCI-E. The SGM6606's internal compensation is optimized for the large output capacitors needed to support the output voltage during large load pulses. The SGM6606 can set the loading current.

The output voltage may be programmed from 3.0V to 5.0V by external resistor divider. Light load switching frequency modulation and low quiescent current maintain high efficiency performance for light load mode conditions.

The output or input current limit can be set by an external current sensing resistor R_{SENSE}. The SGM6606 includes an internal over-voltage protection and a power-good indication. SGM6606 has an internal soft-start circuit to reduce the input peak current.

The SGM6606 is available in Green TDFN-3×3-14L package and is rated over the -40℃ to +85℃ temperature range.

FEATURES

- **2.4V to 5.0V Input Voltage Range**
- **Adjustable 3.0V to 5.0V Output Voltage**
- **Internal Compensation**
- **660kHz Switching Frequency**
- **Synchronous P-Channel MOSFET**
- **Programmable Input or Output Current Limit**
- **Load Current or Input Current Measurement**
- **True Load Disconnect in Shutdown**
- **Reverse Current Block when Enabled**
- **Up to 95% Efficiency**
- **Power-Good Indication**
- **Very Low 50μA No-Load Operating Current**
- **Less than 2μA Shutdown Current**
- **PFM Mode to Keep High Efficiency in Light Load**
- **5.55V Output Over-Voltage Protection**
- **Thermal Shutdown Protection**
- **Output Short-Circuit Protection**
- **Soft-Start to Reduce Input Peak Current**
- **1.8V Control Logic**
- **Available in Green TDFN-3×3-14L Package**
- **-40℃ to +85℃ Operating Temperature Range**

APPLICATIONS

Media Tablets
PCI-Express Cards
PCMCIA Cards
Modems
Wireless Data Cards

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6606	TDFN-3×3-14L	-40℃ to +85℃	SGM6606YTDK14G/TR	SGM 6606DK XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage .... -0.3V to 6V
Supply Voltage on SW, VOUT, EN, FB, $\overline{PG}$
.... -0.3V to 6V
PGND to AGND .... -0.3V to 0.3V
Junction Temperature ....+150℃
Storage Temperature Range.........................-65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM...4000V
MM...200V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ....2.4V to 5.0V
Operating Temperature Range ....-40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

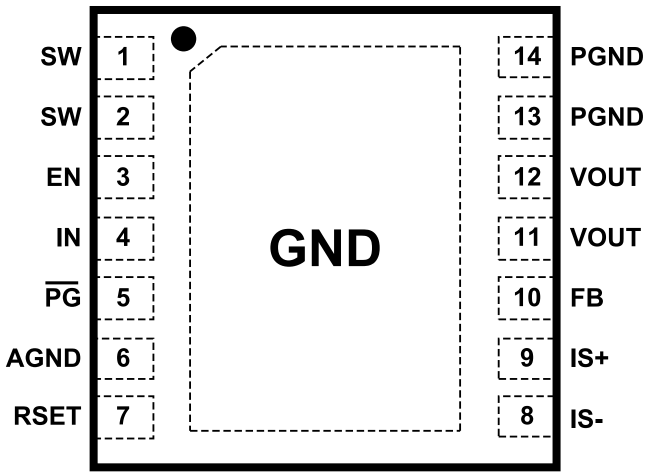
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×3-14L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	SW	Inductor Switching Node. SW is internally connected to the source of the internal low-side N-Channel MOSFET (NMOS), and synchronous high-side P-Channel MOSFET (PMOS). Externally connected to the switching side of the power inductor.
3	EN	Enable Input. A logic high enables the SGM6606 regulator. A logic low forces the SGM6606 into shutdown mode, placing the output into a high-impedance state (true load disconnect) and reducing the quiescent current to less than 1μA.
4	IN	Input Supply. IN powers the analog control circuitry during start-up. Bypass IN to GND with a 10μF or greater ceramic capacitor.
5	$\overline{PG}$	Power-Good Signal (Active Low). $\overline{PG}$ is an open-drain, active-low output. $\overline{PG}$ is pulled low when the feedback voltage exceeds 95% of the target voltage.
6	AGND	Analog Ground. AGND is internally connected to the analog ground of the control circuitry.
7	RSET	RSET is a Monitor Pin. The output voltage at this pin is reflecting the voltage drop across the current sensing resistor R_{SENSE} by a factor of 50.
8	IS-	Current Sense Negative Input. The current limit can be programmed by an external current sensing resistor R_{SENSE}, IS- is connecting to the "negative" side of R_{SENSE}.
9	IS+	Current Sense Positive Input. The current limit can be programmed by an external current sensing resistor R_{SENSE}, IS+ is connecting to the "positive" side of R_{SENSE}.
10	FB	Output Voltage Feedback Pin. FB senses the output voltage for regulation control. For adjustable output version, connect a resistive divider network from the output to FB to GND to set the output voltage accordingly. The FB regulation threshold is 0.6V.
11, 12	VOUT	Output of Step-Up Regulator. VOUT internally connects to the synchronous high-side P-Channel MOSFET.
13, 14	PGND	Power Ground. PGND is internally connected to the source of the low-side N-Channel MOSFET.
Exposed Pad	GND	Power Ground Exposed Pad. Must be connected to ground plane.

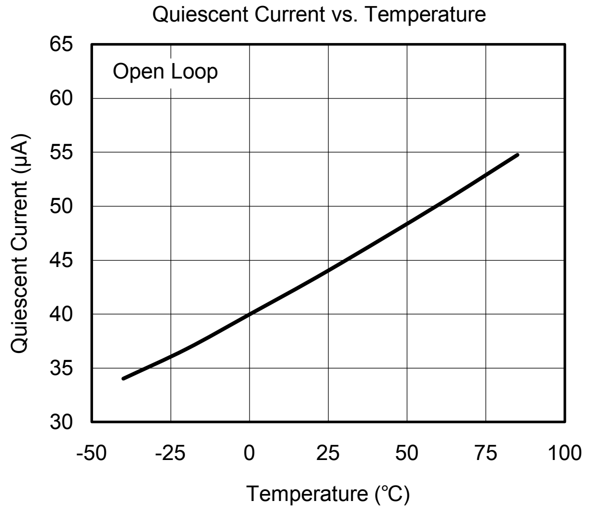
ELECTRICAL CHARACTERISTICS

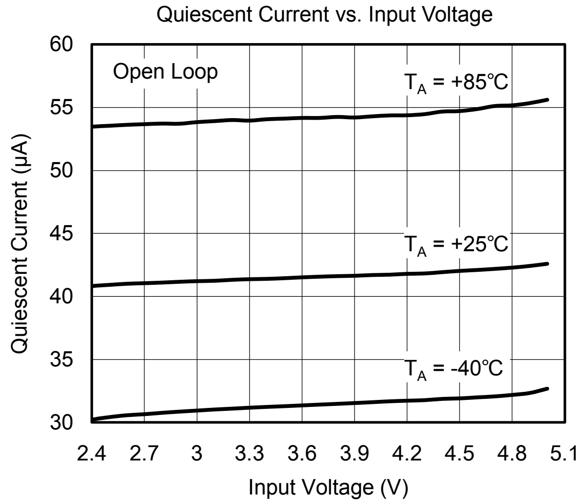
(V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND. T_A = +25℃, unless otherwise noted.)

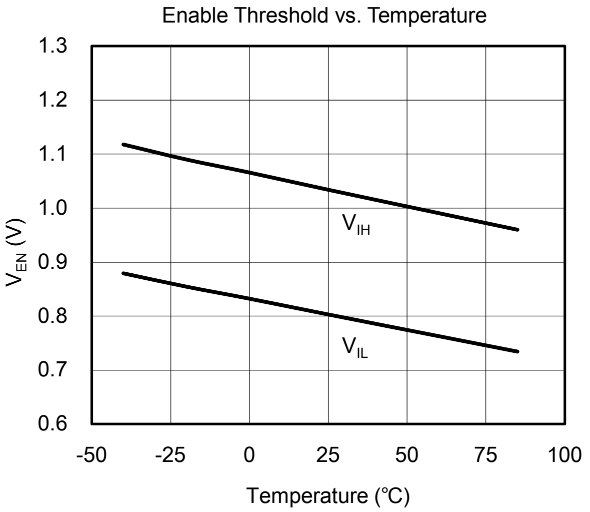
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.4		5.0	V
Minimum Start-Up Voltage	$V_{IN(MIN)}$			2.3		V
Output Voltage Range	V_{OUT}		3.0		5.0	V
Input Under-Voltage Lockout	V_{UVLO}	V_{IN} Rising	2.15	2.25	2.35	V
Quiescent Supply Current	I_Q	No Load Current; Not Switching		50	70	μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = GND, V_{IN} = 5.0V	-2	0.03	2	μA
Feedback Accuracy	V_{FB}	T_A = +25℃, I_{OUT} = 10mA	0.589	0.6	0.611	V
		T_A = -40℃ to +85℃, I_{OUT} = 10mA	0.585	0.6	0.616	
Feedback Leakage Current	I_{FB}	V_{FB} = 0 to 1.0V	-1	0.01	1	μA
Load Regulation	$\Delta V_{OUT}/I_{OUT}$	V_{IN} = 3.3V, V_{OUT} = 3.8V, 0 to 2.5A Load		1		%/A
Line Regulation	$\Delta V_{OUT}/V_{IN}$	V_{IN} = 2.4V to V_{OUT}, I_{OUT} = 10mA		0.3		%/V
Output Over-Voltage Protection Threshold	V_{OVP}		5.25	5.55	5.85	V
Oscillator Frequency	f_{OSC}		560	660	760	kHz
Maximum Duty Cycle	D			90		%
Minimum On-Time	$t_{ON(MIN)}$			80		ns
High-side P-Channel On-Resistance	$R_{ON(PMOS)}$			100		mΩ
Low-side N-Channel On-Resistance	$R_{ON(NMOS)}$			80		mΩ
Low-side Peak Current Limit Threshold	I_{LIMPK}			5		A
Offset Voltage for IS+ and IS- Differential Amplifier	V_{OS}		43	53	63	mV
ENABLE, POWER-GOOD AND START-UP FEATURES						
Logic Input Threshold High for EN	V_{IH}		1.5			V
Logic Input Threshold Low for EN	V_{IL}				0.4	V
EN Input Low Current	I_{EN}	V_{EN} = GND or 5.0V	-1	0.01	5	μA
Power-Good Threshold		FB Rising, Hysteresis = 10%		95		%
$\overline{PG}$ On-Resistance	$R_{\overline{PG}}$	V_{FB} = 0.62V, I_{SINK} = 10μA		135		Ω
THERMAL						
Over-Temperature Shutdown Threshold	T_{SD}	Temperature Rising		150		℃
Over-Temperature Shutdown Hysteresis	T_{HYS}			20		℃

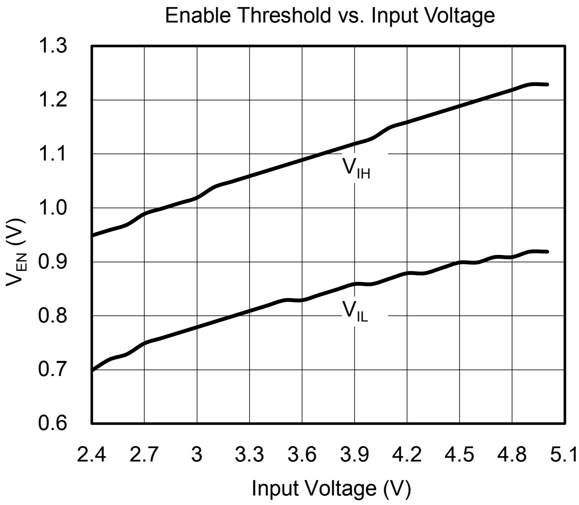
TYPICAL PERFORMANCE CHARACTERISTICS

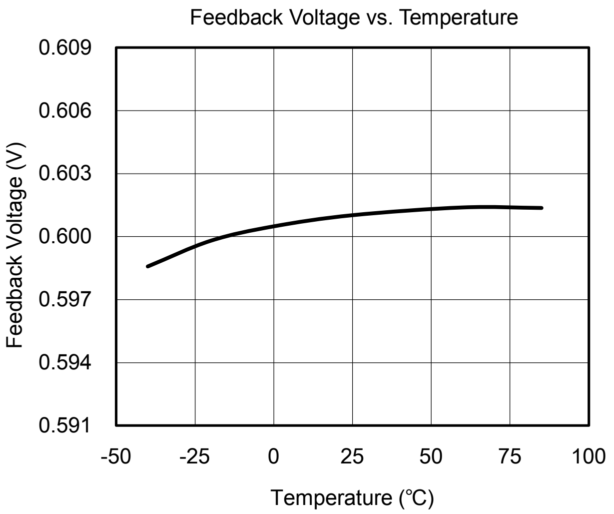
V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND. T_A = +25℃, unless otherwise noted.

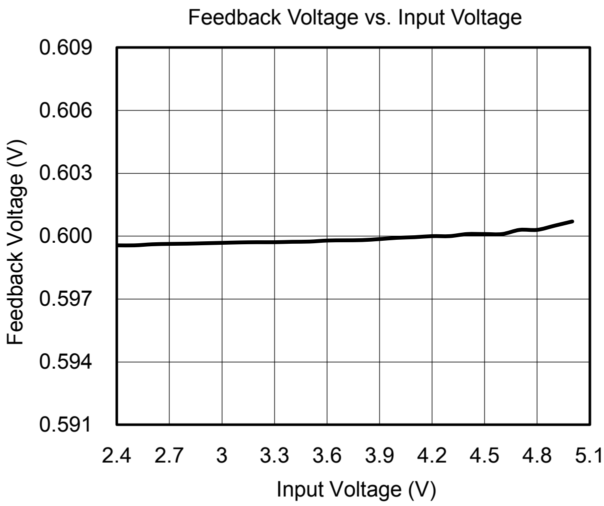








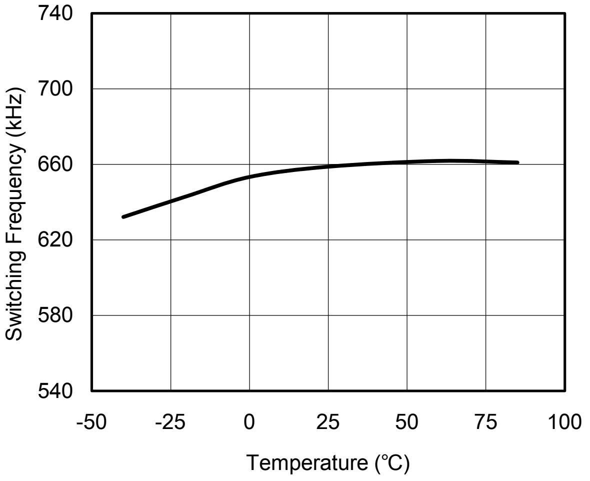




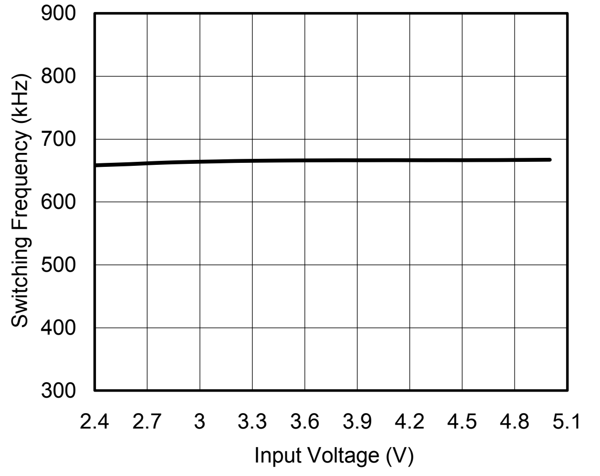
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND. T_A = +25℃, unless otherwise noted.

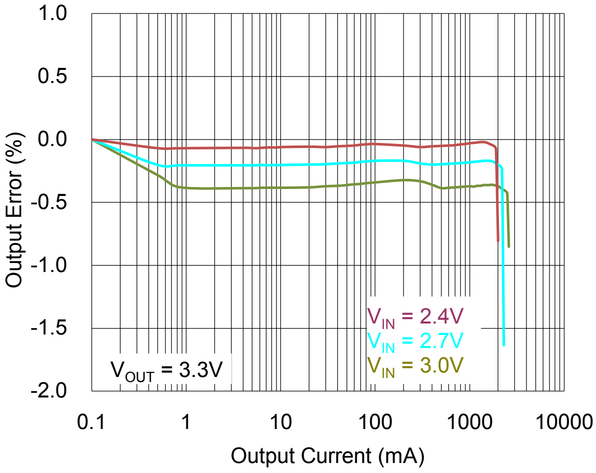
Switching Frequency vs. Temperature



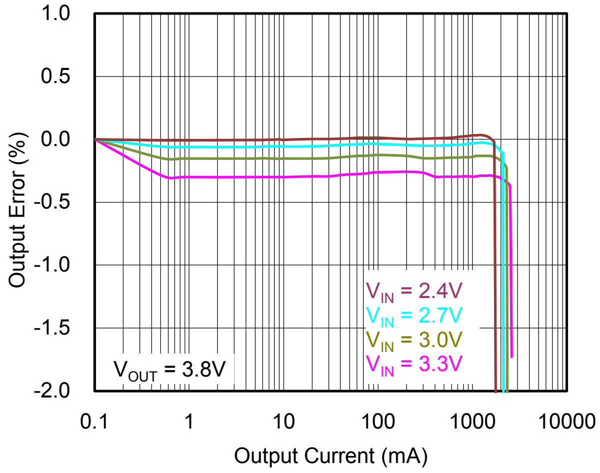
Switching Frequency vs. Input Voltage



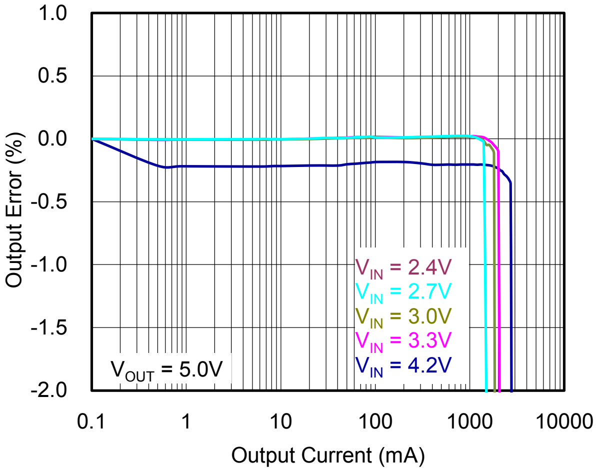
Load Regulation



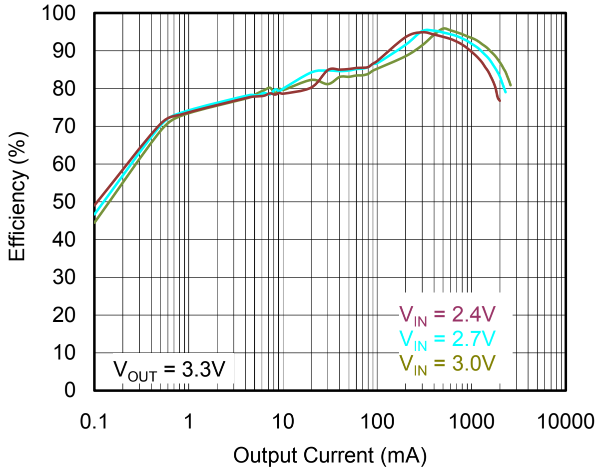
Load Regulation



Load Regulation



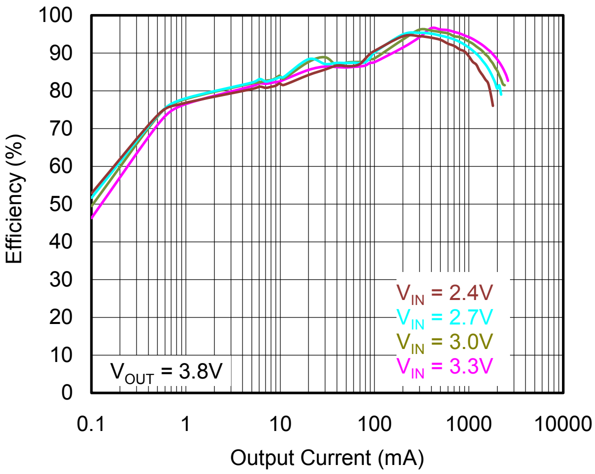
Efficiency vs. Output Current



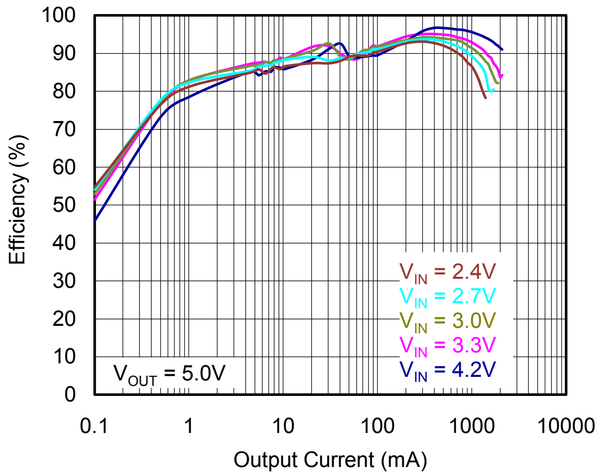
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND. T_A = +25℃, unless otherwise noted.

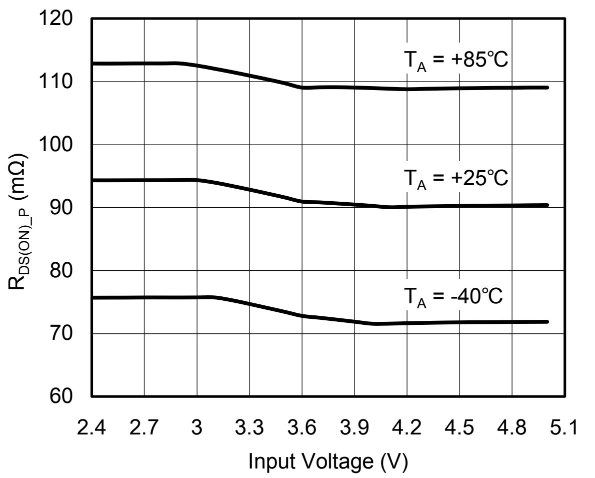
Efficiency vs. Output Current



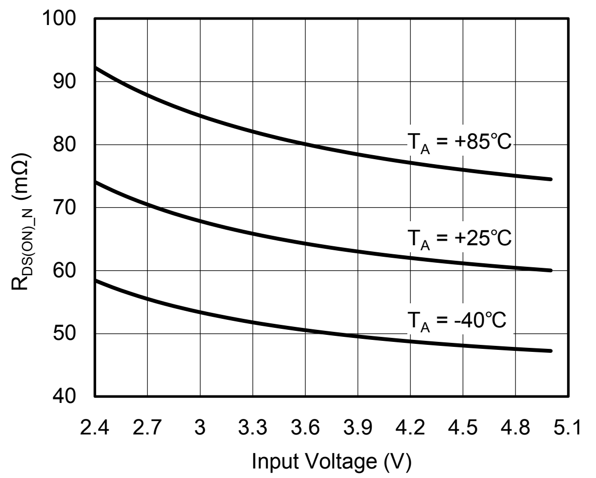
Efficiency vs. Output Current



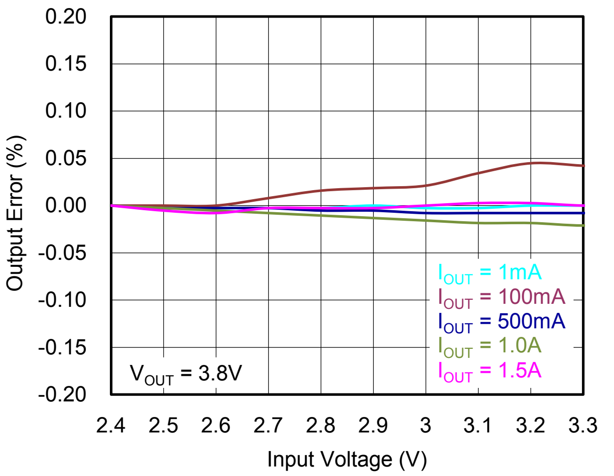
RDS(ON)_P vs. Input Voltage



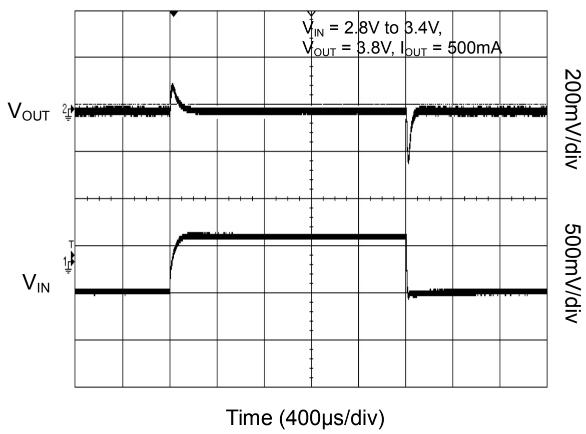
RDS(ON)_N vs. Input Voltage



Line Regulation



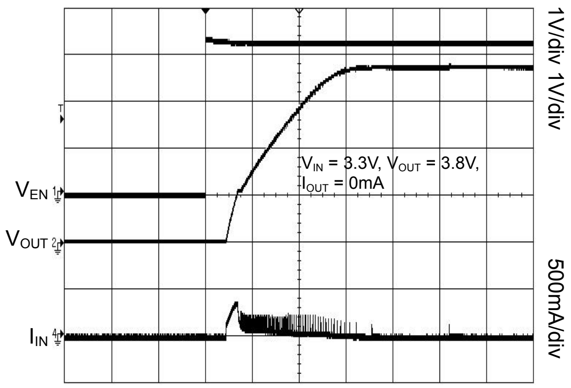
Line Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

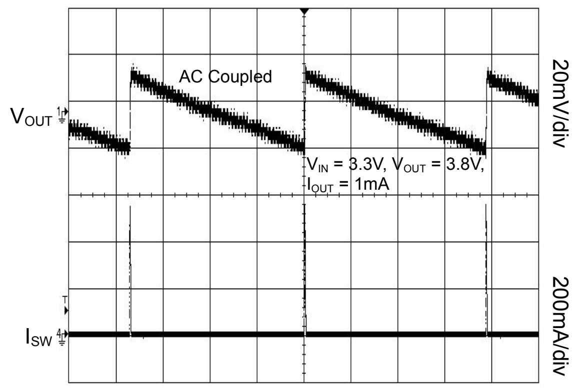
V_{IN} = 3.3V, V_{OUT} = 3.8V, L = 2.2μH, AGND = PGND. T_A = +25℃, unless otherwise noted.

Soft Start



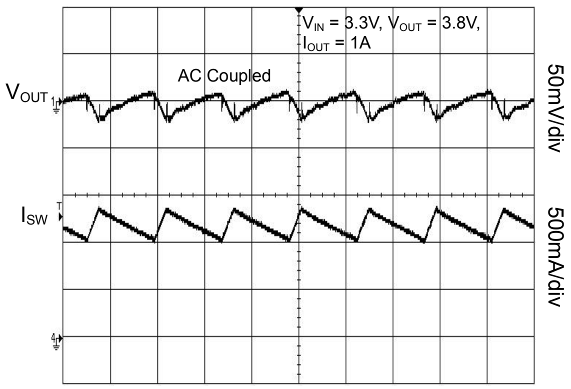
Time (400μs/div)

Output Ripple



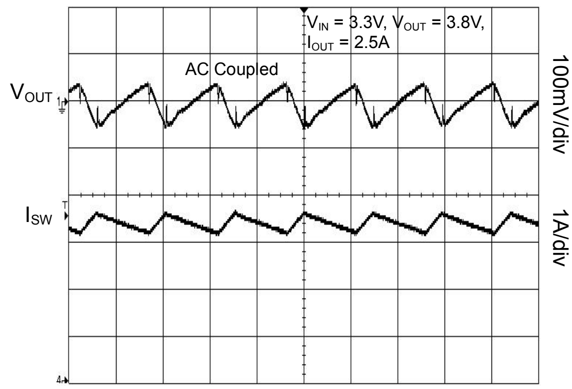
Time (50μs/div)

Output Ripple



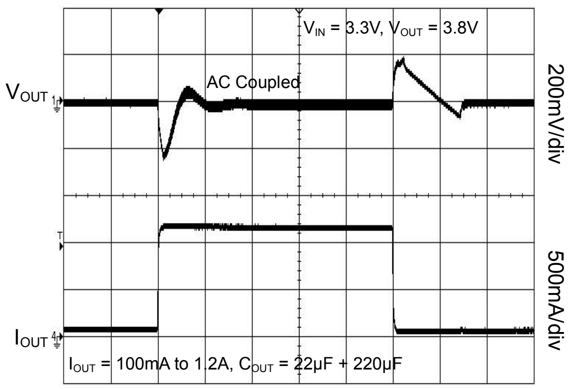
Time (1μs/div)

Output Ripple



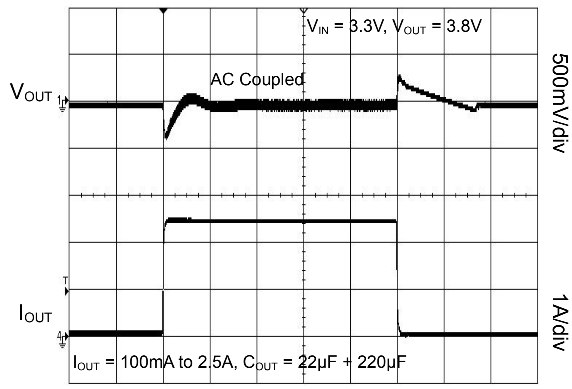
Time (1μs/div)

Load Transient Response



Time (400μs/div)

Load Transient Response



Time (400μs/div)

TYPICAL APPLICATIONS

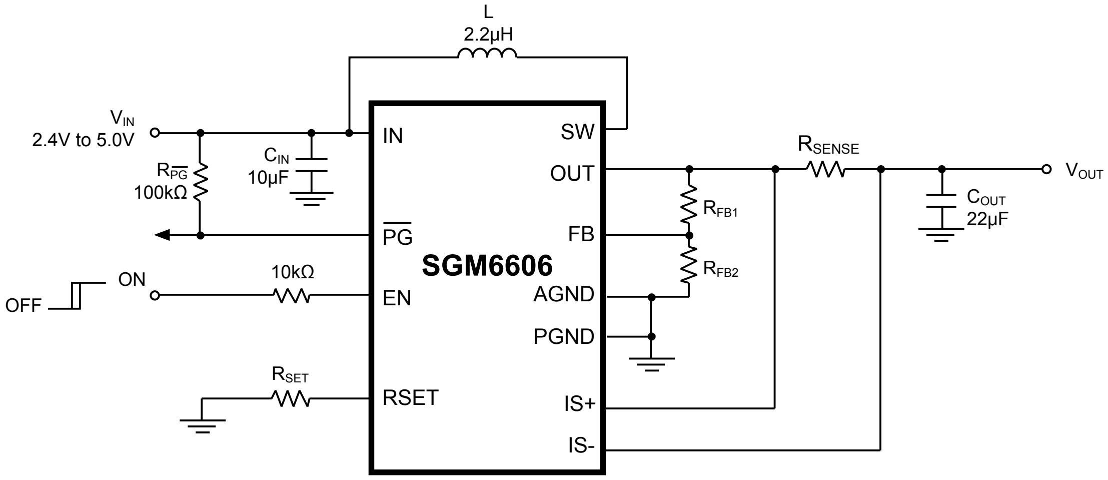


Figure 1. Output Current Limit

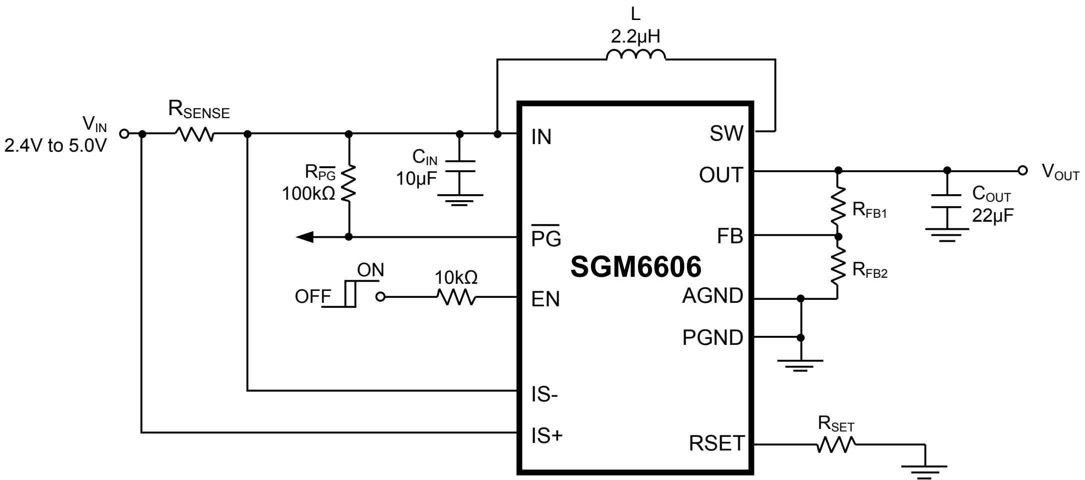
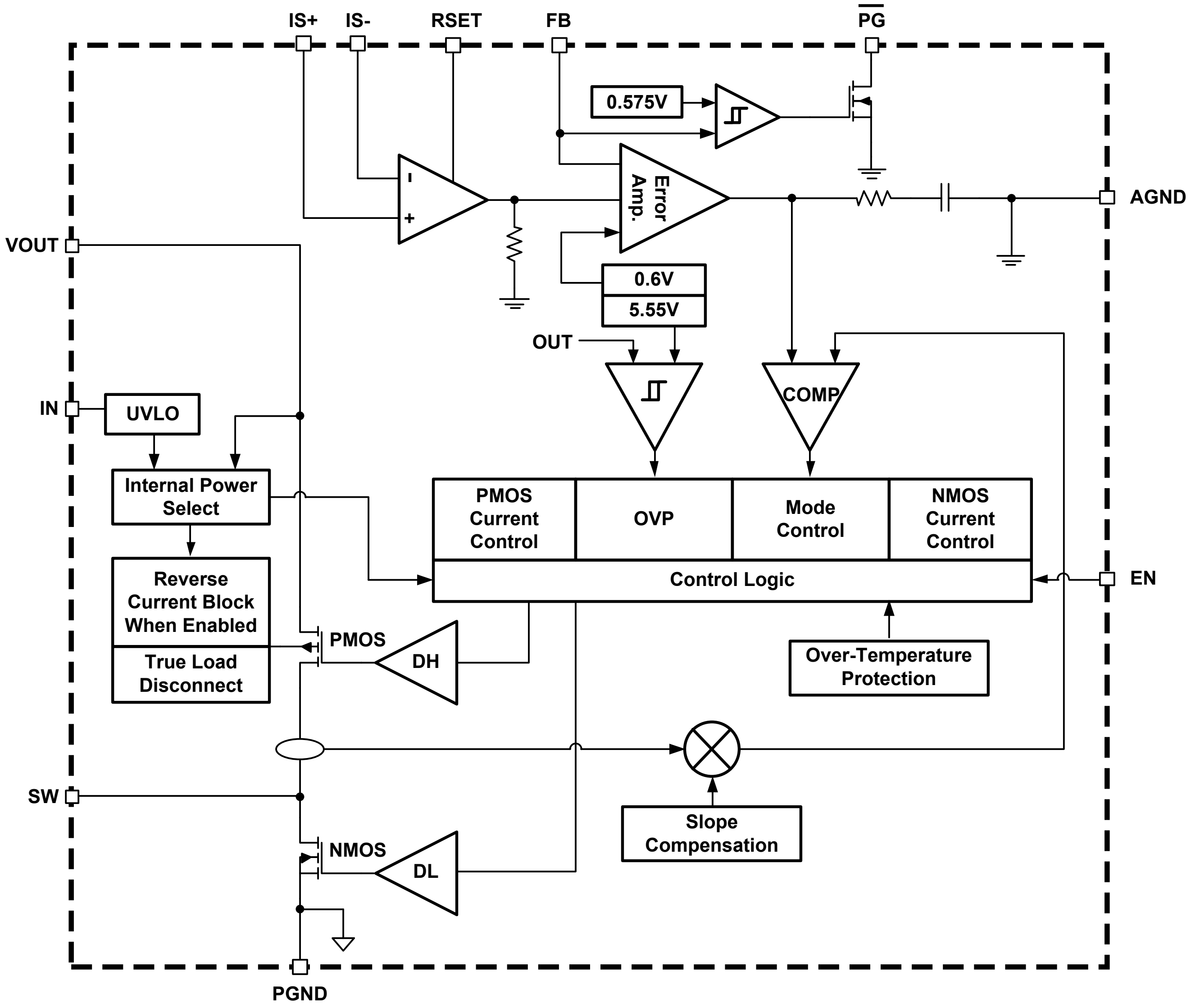


Figure 2. Input Current Limit

FUNCTIONAL BLOCK DIAGRAM



OPERATION

The SGM6606 synchronous step-up converter is designed for boosting battery or interface (such as PCI-E, PCMCIA) power to higher voltage. SGM6606 has a current sense circuit to limit input or output current, current limit is programmable by an external resistor R_{SENSE}.

The 660kHz switching frequency of the SGM6606 facilitates output filter component size reduction for improved power density and reduced overall footprint. It also provides greater bandwidth and improved transient response over other lower frequency step-up converters. The compensation is implemented with three external components - C_{IN}, C_{OUT} and L. Low $R_{DS(ON)}$ synchronous power switches provide high efficiency for heavy load conditions. Switching frequency modulation and low quiescent current maintain high efficiency for light load conditions. In addition to the improved efficiency, the synchronous step-up has the added performance advantage of true load disconnect during shutdown (<2μA shutdown current), reverse current blocking when enabled and short-circuit protection.

PWM Control Scheme with Low Noise and for Light Load

The SGM6606 is a fixed frequency PWM peak current mode control step-up converter. For light load condition, the converter stays in a variable frequency mode to reduce the dominant switching losses. In addition to light load operation, a zero current comparator blocks reverse current in the synchronous P-Channel MOSFET, forcing DCM operation at light load. These controls, along with very low quiescent current, help to maintain high efficiency over the complete load range without increased output voltage ripple during light load conditions.

Shutdown and True Load Disconnect

A typical synchronous step-up converter has a conduction path from the input to the output via the parasitic body diode of the P-Channel MOSFET when the converter shuts down. The SGM6606 design uses a special power selection for the substrate to keep the parasitic body diode in off-state during shutdown and startup. This enables the SGM6606 to provide true load disconnect during shutdown and PMOS inrush current limit at start-up. During the initial PMOS linear mode start-up period, the start-up control circuitry is powered by the input supply pin. When the output voltage of the SGM6606 enters step-up mode ($V_{IN} \approx V_{OUT}$), the step-up control circuitry draws power directly from the output supply to ensure sufficient voltage head-room.

When EN is set to logic low, the step-up converter is forced into shutdown state with less than 2μA input current.

Start-Up Inrush Current Protection

When initially powering up, the load disconnect feature allows the output voltage to be less than the input voltage. In order to avoid large surge current when the regulator is enabled, the SGM6606 operates the synchronous P-Channel MOSFET in a current-limited linear mode to softly charge the large output capacitor. This linear start-up feature effectively limits the input current until the output voltage exceeds the input voltage. After V_{OUT} exceeds V_{IN}, the regulator switches the body diode connection and begins step-up operation.

Programmable Input or Output Current Limit

When the output voltage of the SGM6606 enters step-up mode ($V_{IN} < V_{OUT}$), the maximum between current sense signal and V_{OUT} feedback signal will be selected as the input signal of the error amplifier. The input or output (depending on the location of R_{SENSE}) current limit can be programmed by an external current sensing resistor R_{SENSE}. Please refer to the Application Information section for R_{SENSE} selection.

The V_{OUT} feedback signal is:

$$\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times V_{OUT}$$

Load Current or Input Current Sensing

The output voltage at RSET pin is related to the current sensing result as the following:

$$V_{RSET} = I \times R_{SENSE} \times K$$

Where the factor K is about 50, and I is the current through R_{SENSE}. This output voltage can be used by an external MCU.

OPERATION (continued)

Power-Good Indication

To indicate the output voltage is in regulation, an active low open-drain output pin ($\overline{PG}$) pulls down when the feedback voltage is above 95% of the nominal regulation voltage level. $\overline{PG}$ changes to a high-impedance output if the feedback voltage drops below 85% of the nominal regulation voltage level.

Over-Voltage Protection

The SGM6606's over-voltage protection function prevents the output voltage from exceeding the fixed 5.55V (TYP) over-voltage point, which would exceed the absolute maximum rating of the regulator. If V_{OUT} exceeds 5.55V, the regulator will stop switching until the output voltage drops below 5.5V and FB is below its regulation threshold.

Thermal Shutdown

When the junction temperature exceeds the over-temperature threshold, the SGM6606 thermal protection circuitry shuts down the regulator. Thermal shutdown disables switching to control the current flowing through to avoid any damage of the step-up converter. When the over-temperature fault condition is removed, the step-up recovers regulation automatically.

APPLICATION INFORMATION

R_{SENSE} Selection for Programmable Current Limit

The current limit of the internal power switch is programmable by an external current sensing resistor R_{SENSE}. The maximum current through R_{SENSE} can be calculated by the following equation:

$$I_{LIMIT} = \frac{53mV}{R_{SENSE}}$$

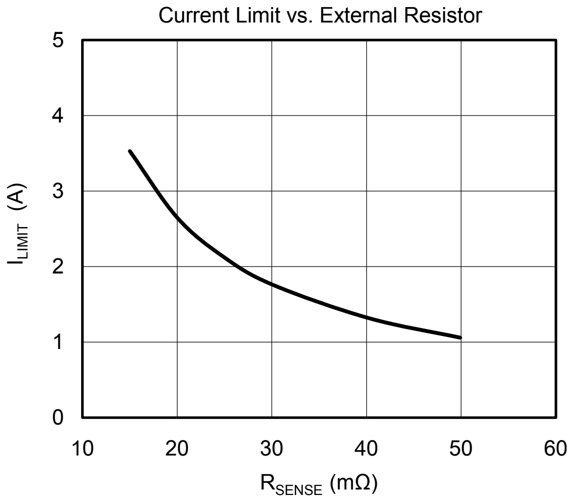


Table 1. Examples of 1% Standard Resistor Value of R_{SENSE}

R_{SENSE} (mΩ)	I_{LIMIT} (A)
15	3.53
20	2.65
24.9	2.13
30.1	1.76
40.2	1.32
49.9	1.06

Output Voltage Programming

The output voltage of the SGM6606 may be programmed from 3.0V to 5.0V with an external resistive voltage divider. Resistors R_{FB1} and R_{FB2} in Figure 1 are used to program the output voltage as shown by the following equation:

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \times R_{FB2}$$

where V_{FB} is the 0.6V feedback reference voltage.

To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the suggested value for R_{FB2} is 100kΩ. Table 2 summarizes the resistor values with R_{FB2} set to 100kΩ for good noise immunity and 6μA increased load current and gives some 1% standard metal film resistor values for R_{FB1} at different output voltage settings.

Table 2. 1% Standard Resistor Examples for Different Output Voltages

V_{OUT} (V)	R_{FB2} = 100kΩ R_{FB1} = (kΩ)
3	402
3.3	453
3.6	499
3.8	536
4.2	604
4.5	649
5	732

Inductor Selection

The SGM6606 is designed to operate with a 2.2μH inductor for all input/output voltage combinations. For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

Input Capacitor

Select a low ESR ceramic capacitor with a value of at least 10μF as the input capacitor. Place the input capacitor as close to the IN and PGND pins as possible in order to minimize the stray resistance from the converter to the input power source.

Output Capacitor

The output capacitor provides energy to the load when the high-side MOSFET is switched off. The output capacitance together with the boost switching frequency, duty cycle, and load current value determine the capacitive output voltage ripple when the boost operation is in the continuous PWM state.

$$\Delta V_{OUT} = \frac{I_{OUT} \times D}{C_{OUT} \times f_{SW}}$$

APPLICATION INFORMATION (continued)

where D is the duty ratio of low-side MOSFET turn-on time divided by the switching period. It is calculated using the equation:

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

The output capacitor's ESR increases the output ripple by I_{OUT} × ESR. The total output ripple is:

$$\Delta V_{OUT} = I_{OUT} \times ESR + \frac{I_{OUT} \times D}{C_{OUT} \times f_{SW}}$$

So the minimum recommended output capacitor value may be determined by:

$$C_{OUT} \geq \frac{I_{OUT} \times D}{\Delta V_{OUT} - I_{OUT} \times ESR} \times \frac{1}{f_{SW}}$$

High Load Pulse Application

Together with a large value output capacitor or supercap, the SGM6606 can support a higher load pulse in lower input current limited applications such as GSM burst mode in WCDMA, Edge, GPRS and TD-SCDMA applications. The large capacitance is determined by NMOS peak current limit, inductor current ripple, V_{IN}, V_{OUT}, load pulse high current level and elapsed time. The capacitor value can be calculated using the following three steps as follows:

First calculate the SGM6606's load-on current from the expected I_{LIM}. Assume the input current equals I_{LIM} because the inductor current ripple is low enough when compared to the input current:

$$I_{OUT\_BOOST} = \frac{V_{IN} \times I_{LIM} \times \eta}{V_{OUT}}$$

Second, calculate the maximum current the large capacitor C_{OUT} should provide:

$$I_{COUT} = I_{LOAD\_PEAK} - I_{OUT\_BOOST}$$

Finally, derive the C_{OUT} at a certain load-on period t_{ON}:

$$C_{OUT} = \frac{I_{COUT} \times t_{ON}}{\Delta V_{OUT}}$$

To consider the real tantalum capacitor having 20% tolerance, the selected capacitance should be 20% higher than the calculated value. Example: A 2.0A, 217Hz 12.5% duty cycle load pulse is applied on 3.8V V_{OUT} at 3.3V V_{IN}. An input peak current limit of 2.4A and a V_{OUT} drop of less than 450mV are required. Under these conditions, with 90% efficiency, the SGM6606's output current is:

$$I_{OUT\_BOOST} = \frac{3.3 \times 2.4 \times 90\%}{3.8} = 1.876A$$

The maximum current necessary for the large capacitor value is:

$$I_{COUT} = 2.0 - 1.876 = 0.124A$$

t_{ON} is 593μs for a 217Hz 12.5% duty cycle load pulse. Considering a 20% capacitance tolerance, the minimum capacitance should be 220μF. Figure 3 shows the SGM6606 operating waveform under a 593μs 2.0A load pulse with a 220μF capacitor as C_{OUT}, as well as a 22μF ceramic capacitor to closely filter the output voltage.

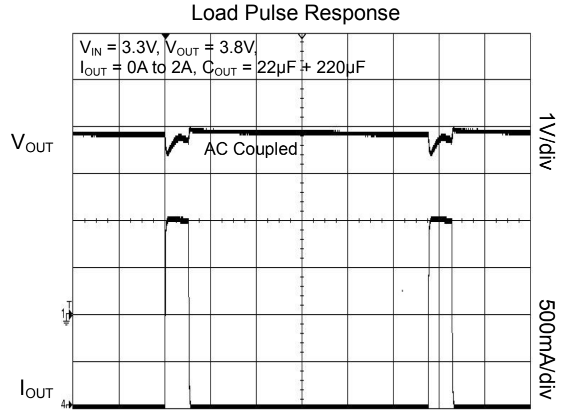


Figure 3. SGM6606 Operation Waveform When 217Hz 593μs 2.0A Load Pulse is Applied

Layout Guidance

For best performance of the SGM6606, the following guidelines should be followed when designing the PCB layout:

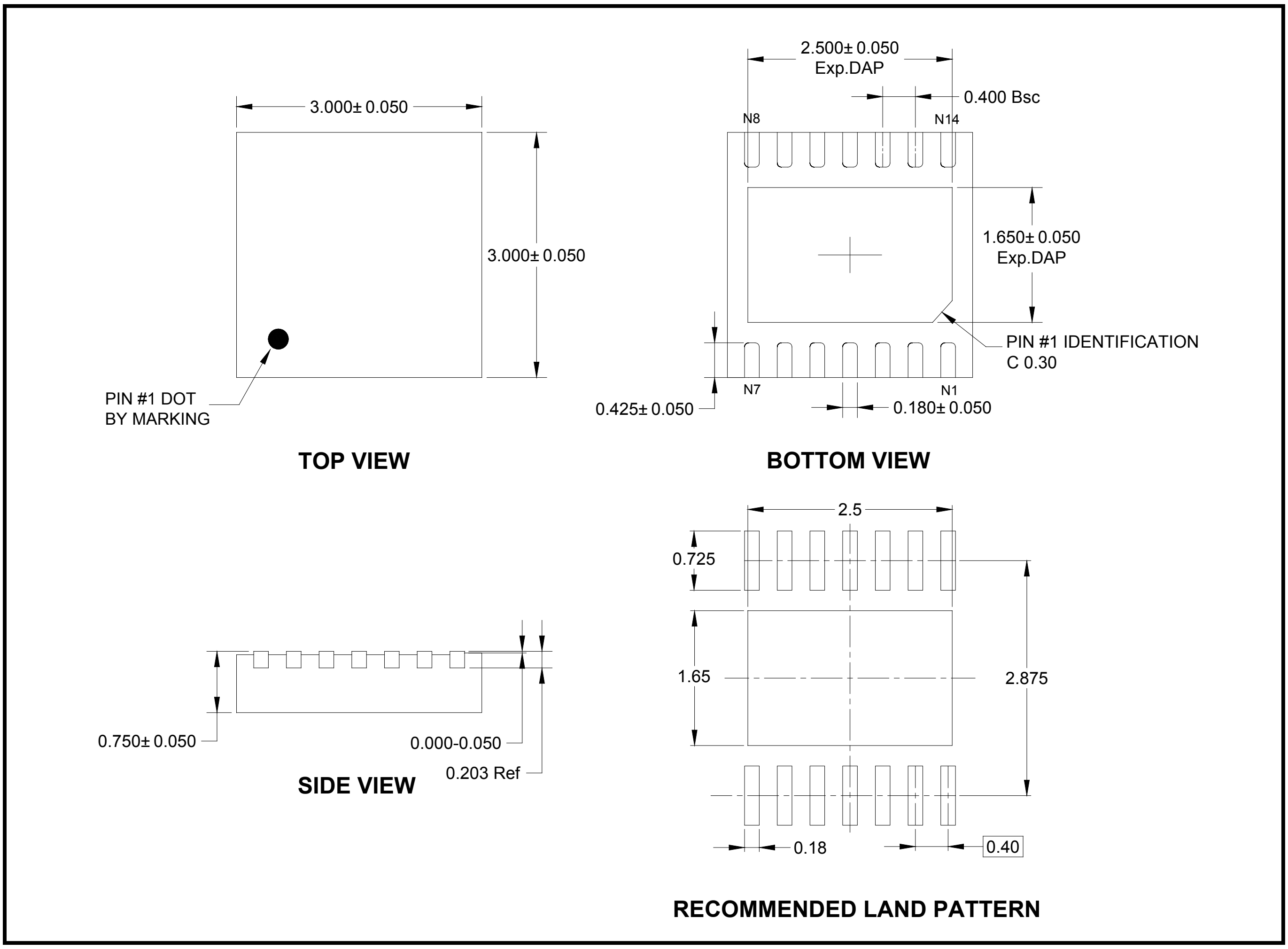
1. Make the power trace as short and wide as possible, including the input/output power lines and switching node, etc.

2. Connect the analog and power grounds together with a single short line and connect all low current loop grounds to analog ground to decrease the power ground noise on the analog ground and achieve better load regulation.

3. For good power dissipation, connect the exposed pad under the package to the top and bottom ground planes by PCB pads.

PACKAGE OUTLINE DIMENSIONS

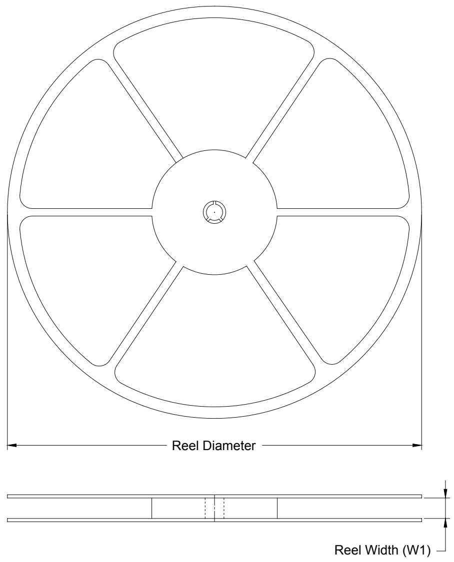
TDFN-3×3-14L



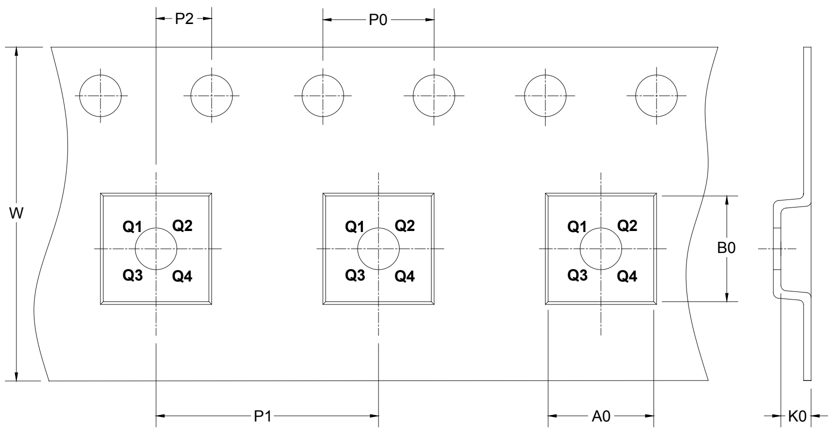
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



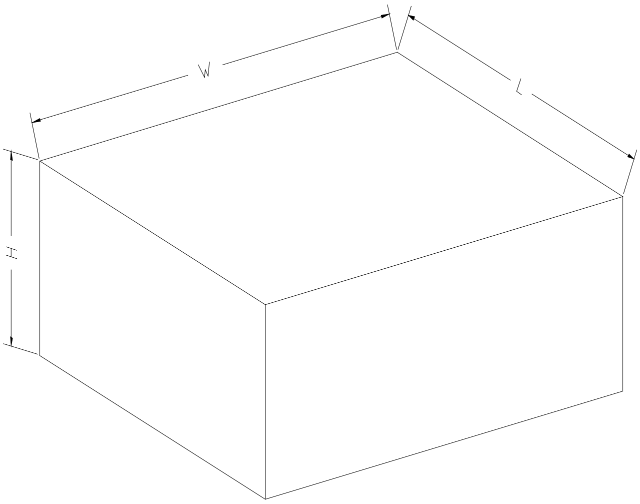
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-14L	13″	12.4	3.35	3.35	1.13	4.00	8.00	2.00	12.00	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002