SGM6518
High Speed, 16-Input, 8-Output Crosspoint Switch

GENERAL DESCRIPTION

The SGM6518 crosspoint switch provides flexible options for signal switching applications. The 16 inputs can be routed to any of 8 outputs. Each input can be routed to one or more outputs, but only one input can be routed to any one output. More than one output can connect to the same input channel for one-to-many routing. The input to output routing is controlled via a serial interface. Many SGM6518 devices can be used independently or constructed as daisy-chain controlled serial interface.

For analog signal switching application, 8 outputs can be 8 single outputs or 4 differential outputs depending on configuration. Crosspoint structure can reduce PCB complexity.

The resistance profile of SGM6518 is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. For video application, SGM6518 supports up to 1080p or VGA video.

The SGM6518 is available in Green LQFP-7×7-32L package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Supply Voltage Range: 2.7V to 5.5V**
- **Power On Reset and All Inputs are Disconnected with All Outputs**
- **16 × 8 Crosspoint Switch**
- **One-to-One or One-to-Many Output Switching**
- **Supports Bidirectional Transmission**
- **Serial Digital Interface**
- **Support Daisy-Chain Connection**
- **Supports WUXGA (1920 × 1200) Video**
- **Supports Low Noise Analog Signal Switching**
- **-3dB Bandwidth: 250MHz**
- **Very Low Crosstalk to Support Audio Signal**
- **1.8V Logic Control I/O**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green LQFP-7×7-32L Package**

APPLICATIONS

Video and Audio Matrix Switching System
Audio and Video Receiver
Automotive Entertainment System
Data Acquisition and Control System

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6518	LQFP-7×7-32L	-40℃ to +85℃	SGM6518YLFA32G/TY	SGM6518 YLFA32 XXXXX	2 Tray (500pcs)

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage ..... -0.3V to 6V
Analog and Digital I/O .....-0.3V to V_{CC} + 0.3V
Continuous Current IN, OUT..... 10mA
Junction Temperature .....150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering 10 sec) .....260℃
ESD Susceptibility
HBM.....7000V
MM.....300V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .....2.7V to 5.5V
Operating Temperature Range .....-40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

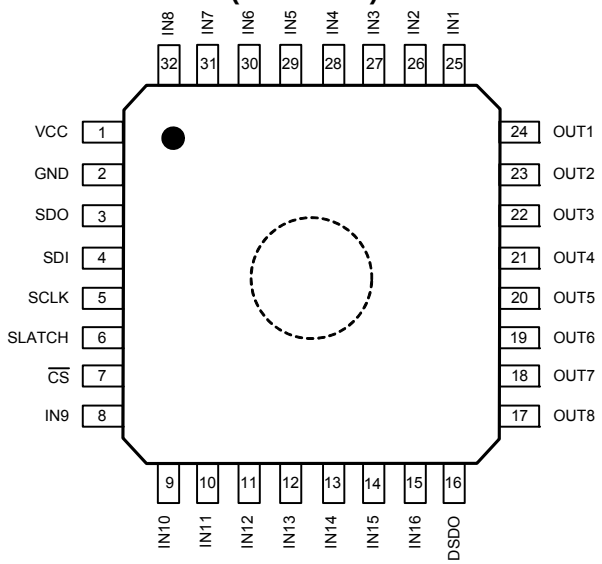
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION

(TOP VIEW)



LQFP-7×7-32L

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	VCC	Positive Power Supply.
2	GND	Ground.
3	SDO	Serial Data Output.
4	SDI	Serial Data Input.
5	SCLK	Serial Clock.
6	SLATCH	Serial Latch. Serial data is latched into SGM6518 on rising edge of SLATCH.
7	$\overline{CS}$	Chip Select for Serial Interface. If $\overline{CS}$ = "High", serial interface doesn't respond to external write or read operation; if $\overline{CS}$ = "Low", serial interface responds to write or read operation.
8	IN9	Input. Channel 9.
9	IN10	Input. Channel 10.
10	IN11	Input. Channel 11.
11	IN12	Input. Channel 12.
12	IN13	Input. Channel 13.
13	IN14	Input. Channel 14.
14	IN15	Input. Channel 15.
15	IN16	Input. Channel 16.
16	DSDO	DSDO for Daisy-Chain Connection. It can be tied to SDI of another SGM6518 to enable daisy-chaining of multiple devices. DSDO's function is the same as SDO.
17	OUT8	Output. Channel 8.
18	OUT7	Output. Channel 7.
19	OUT6	Output. Channel 6.
20	OUT5	Output. Channel 5.
21	OUT4	Output. Channel 4.
22	OUT3	Output. Channel 3.
23	OUT2	Output. Channel 2.
24	OUT1	Output. Channel 1.
25	IN1	Input. Channel 1.
26	IN2	Input. Channel 2.
27	IN3	Input. Channel 3.
28	IN4	Input. Channel 4.
29	IN5	Input. Channel 5.
30	IN6	Input. Channel 6.
31	IN7	Input. Channel 7.
32	IN8	Input. Channel 8.

TYPICAL APPLICATION CIRCUITS

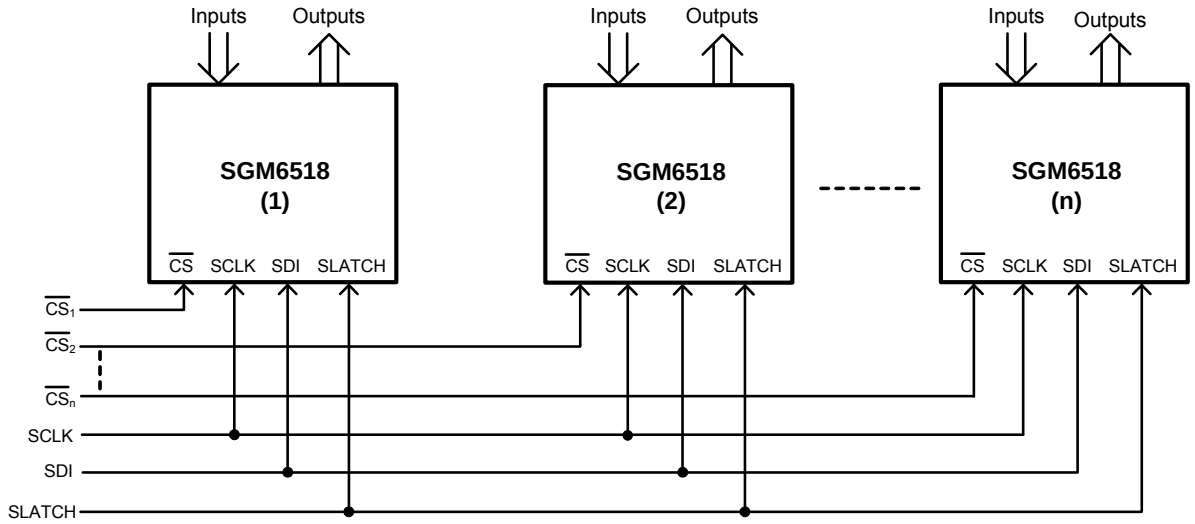


Figure 1. Independent Connection

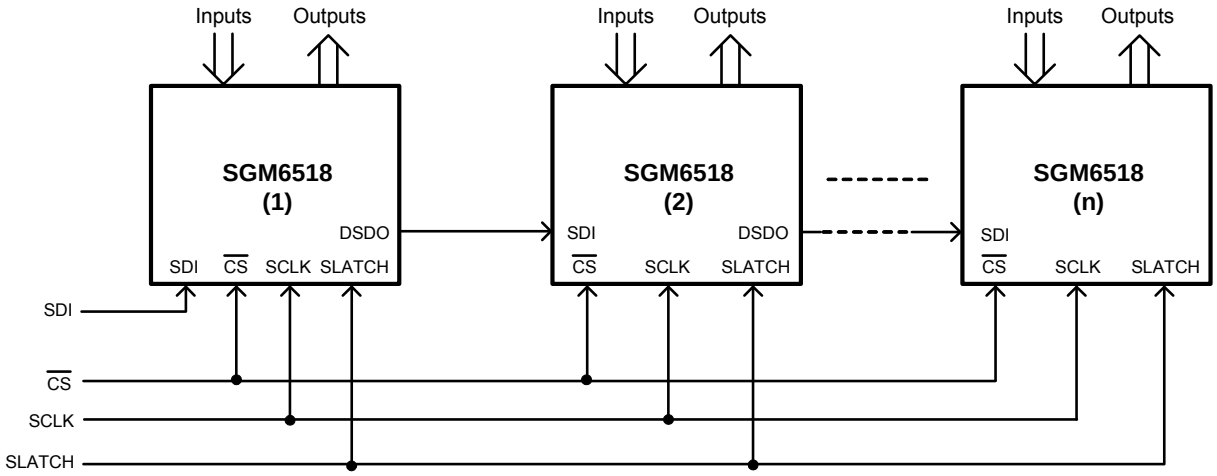


Figure 2. Daisy-Chain Connection

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, Full = -40℃ to +85℃. Typical values are at V_{CC} = +5.0V, T_A = +25℃, unless otherwise noted.)

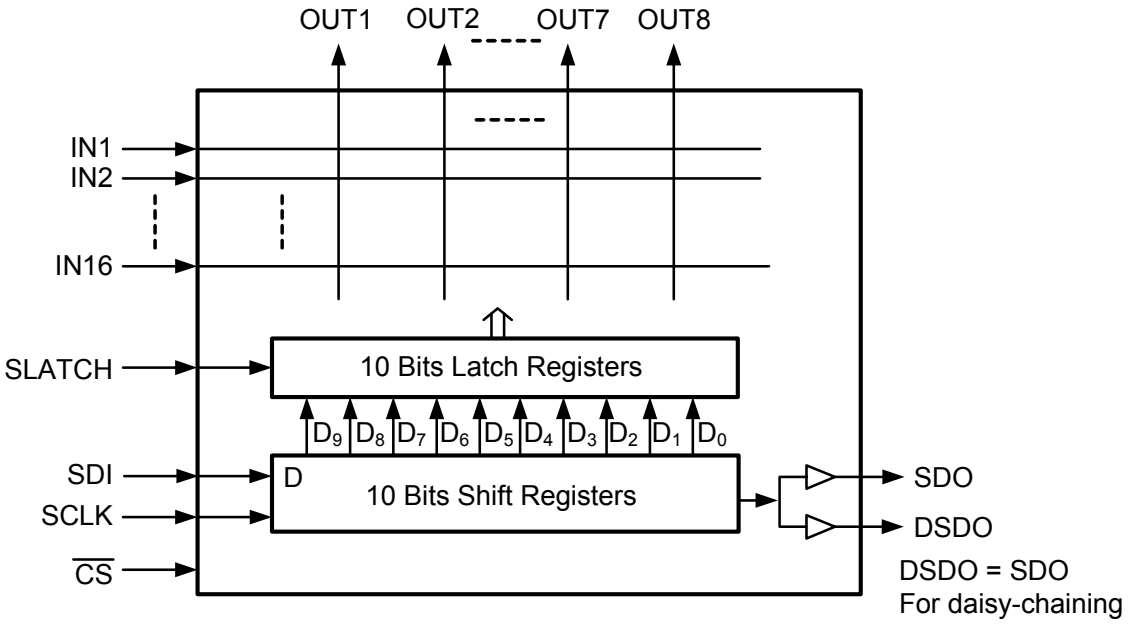
PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{IN}, V_{OUT}			Full	0		V_{CC}	V
Supply Voltage Range	V_{CC}			Full	2.7		5.5	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		28	36	Ω
				Full			42.5	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 4.5V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		3.5	6.2	Ω
				Full			7.5	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 4.5V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		7	12	Ω
				Full			13	
Source OFF Leakage Current	I_{OFF}	V_{CC} = 5.5V, V_{IN} = 4.5V/1V, V_{OUT} = 1V/4.5V		Full			1	μA
Channel ON Leakage Current	I_{ON}	V_{CC} = 5.5V, V_{OUT} = 1V/4.5V, V_{IN} = 1V/4.5V or floating		Full			1	μA
Supply Current	I_{CC}	V_{CC} = 5.5V		Full		10	22	μA
LOGICAL LEVEL OF $\overline{CS}$, SDI, SCLK AND SLATCH								
High-Level Input Voltage	V_{IH}			Full	1.8			V
Low-Level Input Voltage	V_{IL}			Full			0.6	V
Input Leakage Current	I_{DIN}	V_{CC} = 5.5V, V_{DIN} = 5.5V		Full			2	μA
OUTPUT ABILITY OF SDO AND DSDO								
High-Level Output Voltage	V_{OH}	V_{CC} = 5V, I_{SOURCE} = +10mA		+25℃	4.8			V
Low-Level Output Voltage	V_{OL}	V_{CC} = 5V, I_{SINK} = -10mA		+25℃			0.16	V
DYNAMIC CHARACTERISTICS								
Break-Before-Make Time Delay	t_D	V_{IN} = 3V, R_L = 50Ω, C_L = 35pF		+25℃		7		ns
Charge Injection	Q	V_G = GND, R_G = 0Ω, C_L = 1.0nF, Q = C_L × V_{OUT}		+25℃		6		pC
Off Isolation	O_{ISO}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-78		dB
			10MHz	+25℃		-58		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
Channel-to-Channel Crosstalk	X_{TALK}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-78		dB
			10MHz	+25℃		-58		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
-3dB Bandwidth	BW	V_{IN} = 1V_{PP}		+25℃		250		MHz
Channel ON Capacitance	C_{ON}	f = 1MHz		+25℃		50		pF
Digital Input Capacitance	C_{DIN}	V_{CC} = 5V		+25℃		6		pF

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, Full = -40℃ to +85℃. Typical values are at V_{CC} = +3.0V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{IN}, V_{OUT}			Full	0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 2.7V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		65	83	Ω
				Full			88	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 2.7V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		4.5	10.5	Ω
				Full			12	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 2.7V, 0V ≤ V_{IN} ≤ V_{CC}, I_{OUT} = -10mA		+25℃		36	50.5	Ω
				Full			53	
Source OFF Leakage Current	I_{OFF}	V_{CC} = 3.6V, V_{IN} = 3.3V/0.3V, V_{OUT} = 0.3V/3.3V		Full			1	μA
Channel ON Leakage Current	I_{ON}	V_{CC} = 3.6V, V_{OUT} = 0.3V/3.3V, V_{IN} = 0.3V/3.3V or floating		Full			1	μA
Supply Current	I_{CC}	V_{CC} = 3.6V		Full		6	12	μA
DYNAMIC CHARACTERISTICS								
Break-Before-Make Time Delay	t_D	V_{IN} = 1.5V, R_L = 50Ω, C_L = 35pF		+25℃		10		ns
Charge Injection	Q	V_G = GND, R_G = 0Ω, C_L = 1.0nF, Q = C_L × V_{OUT}		+25℃		6		pC
Off Isolation	O_{ISO}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-78		dB
			10MHz	+25℃		-58		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
Channel-to-Channel Crosstalk	X_{TALK}	V_{IN} = 0dBm, R_L = 75Ω	1MHz	+25℃		-78		dB
			10MHz	+25℃		-58		
		V_{IN} = 2V_{PP}, R_L = 600Ω	1kHz	+25℃		-110		
			20kHz	+25℃		-85		
-3dB Bandwidth	BW	V_{IN} = 1V_{PP}		+25℃		250		MHz
Channel ON Capacitance	C_{ON}	f = 1MHz		+25℃		50		pF
Digital Input Capacitance	C_{DIN}	V_{CC} = 3V		+25℃		6		pF

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Serial Digital Interface

The SGM6518 uses a serial interface to program the configuration registers. The serial interface uses three signals (SCLK, SDI, and SLATCH) for programming the SGM6518, while a fourth signal (SDO or DSDO) enables optional daisy-chaining of multiple devices. The serial clock can run at up to 5MHz (5Mbits/s).

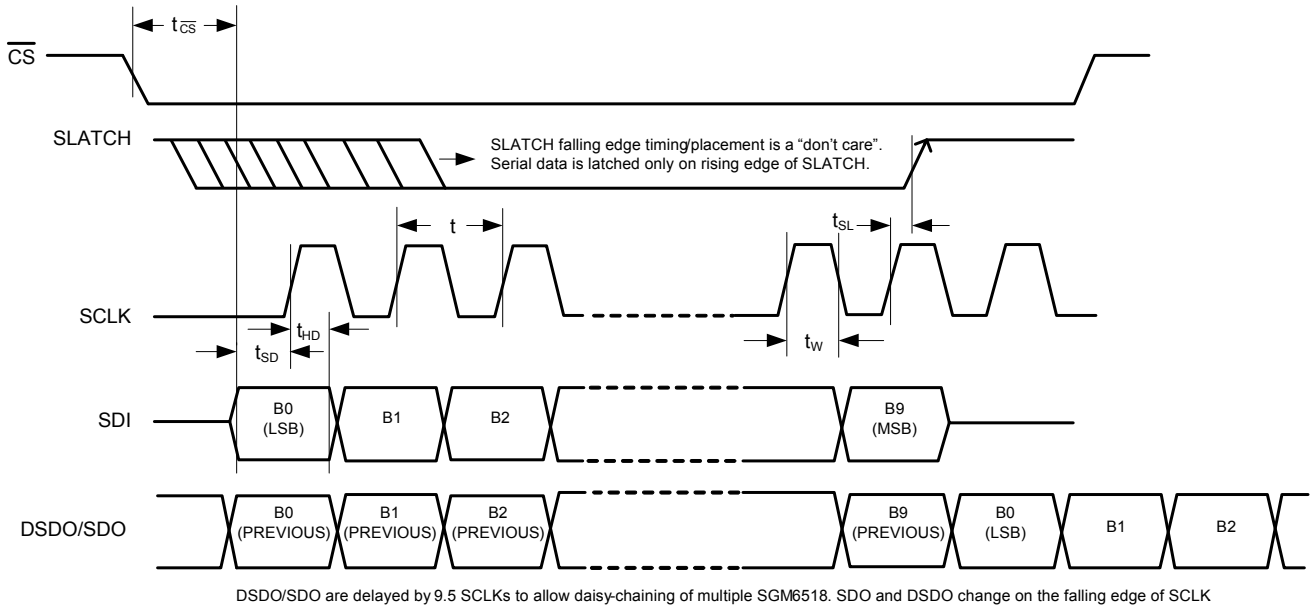
$\overline{CS}$ must be changed from "High" to "Low" before serial interface operation, and kept in "Low" status. After operation is finished, $\overline{CS}$ will be changed from "Low" to "High". When chip is selected, data on the SDI pin is shifted into a 10-bit shift register on the rising edge of the SCLK signal (this is continuously done regardless of the state of the SLATCH signal). The LSB (Bit 0) is loaded first and the MSB (Bit 9) is loaded last (see the Serial Timing Diagram on page 8). After all 10 bits of data have been loaded into the shift register, the rising edge of SLATCH updates the internal registers.

While the SGM6518 has SDO and DSDO pins, they do not have a register readback feature. The data on the SDO and DSDO pins are an exact replica of the incoming data on the SDI pin, delayed by 9.5 SCLKs (an input bit is latched on the rising edge of SCLK, and is output on SDO and DSDO on the falling edge of SCLK after 9.5 SCLKs). Multiple SGM6518's can be daisy-chained by connecting the DSDO of one to the SDI of the other, with SCLK and SLATCH common to all the daisy-chained parts. After all the serial data is transmitted (10 bits × N devices = 10 × N SCLKs), the rising edge of SLATCH will update the configuration registers of all N devices simultaneously.

The Serial Timing Diagram on page 8 and Table 1 show the timing requirements for the serial interface.

DETAILED DESCRIPTION

Serial Timing Diagram



DSDO/SDO are delayed by 9.5 SCLKs to allow daisy-chaining of multiple SGM6518. SDO and DSDO change on the falling edge of SCLK

Table 1. Serial Timing Parameters

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
t	≥ 200ns	SCLK Period.
t_W	0.5 × t	Clock Pulse Width.
t_{SD}	≥ 20ns	Data Setup Time.
t_{HD}	≥ 20ns	Data Hold Time.
t_{SL}	≥ 20ns	Final SCLK Rising Edge (latching B9) to SLATCH Rising Edge.
$t_{\overline{CS}}$	≥ 20ns	$\overline{CS}$ Setup Time. $\overline{CS}$ must change from "High" to "Low" before serial interface operation.

Programming Mode

The SGM6518 is configured by a series of 10-bit serial control words. The two MSBs (B9 and B8) of each serial word determine the basic command:

Table 2. Command Format

B9	B8	COMMAND	NUMBER OF WRITES
0	0	Chip Global Reset (All input and all output will be disconnected).	1
0	1	Input/Output Connection Mapping (Maps input channels to output channels).	8 (1 output channel per write)
1	0	Broadcast (Broadcasts selected channel to all output channels).	1
1	1	Reserved.	

DETAILED DESCRIPTION

Mapping Input to Output Mode

Inputs are mapped to their desired outputs using the input/output control word. Its format is:

Table 3. INPUT/OUTPUT Mapping Control Word

B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	ON/OFF	I_3	I_2	I_1	I_0	O_2	O_1	O_0

I_3:I_0 form the 4-bit word indicating the selected input channel (1 to 16), and O_2:O_0 determine the selected output channel (1 to 8) to which that input channel will be mapped. One input can be mapped to one or multiple outputs. To fully program the SGM6518, 8 INPUT/OUTPUT mapping control words must be transmitted - one for each output channel.

B7 = “1”, selected input channel will be connected with selected output.
B7 = “0”, selected input channel will be disconnected with selected output.

Global Reset Mode

Global reset is used to disconnect all inputs and outputs quickly.

Table 4. Chip Global Reset Control Word

B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	X	X	X	X	X	X	X	X

Once global reset word is latched into SGM6518, all inputs will disconnect with all outputs at once.

Broadcast Mode

The selected input channel will be connected to all 8 output channels in this mode.

Table 5. Broadcast Mode Control Word

B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	0	X	I_3	I_2	I_1	I_0	X	X	X

Once broadcast mode control word is latched into SGM6518, the selected input channel will be connected with all 8 output channels at once.

APPLICATION NOTES

Layout Considerations

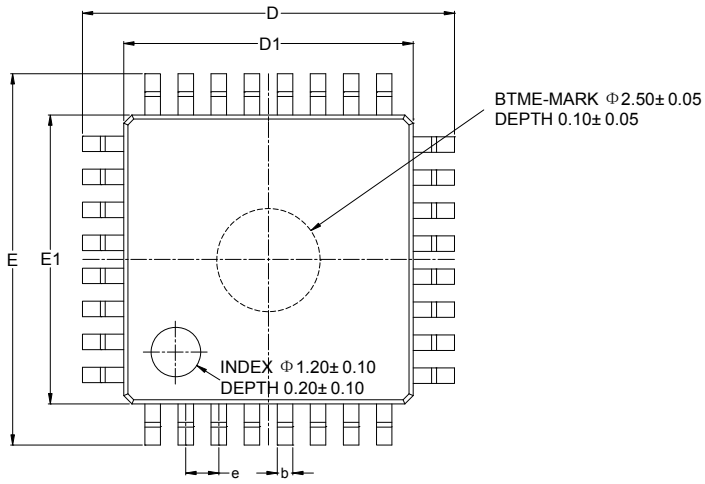
General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed on the right.

Recommended Routing/Layout Rules

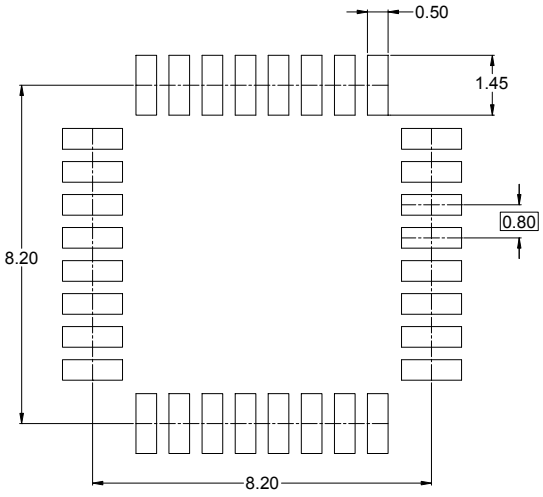
- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10μF and 0.1μF ceramic power supply bypass capacitors.
- Place the 0.1μF capacitor within 0.1 inches of the device power pin.
- Place the 10μF capacitor within 0.75 inches of the device power pin.
- For multilayer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body by at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

PACKAGE OUTLINE DIMENSIONS

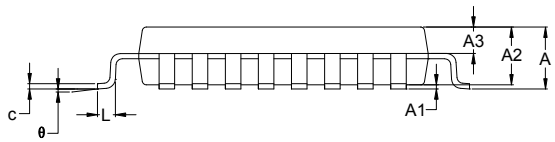
LQFP-7×7-32L



TOP VIEW



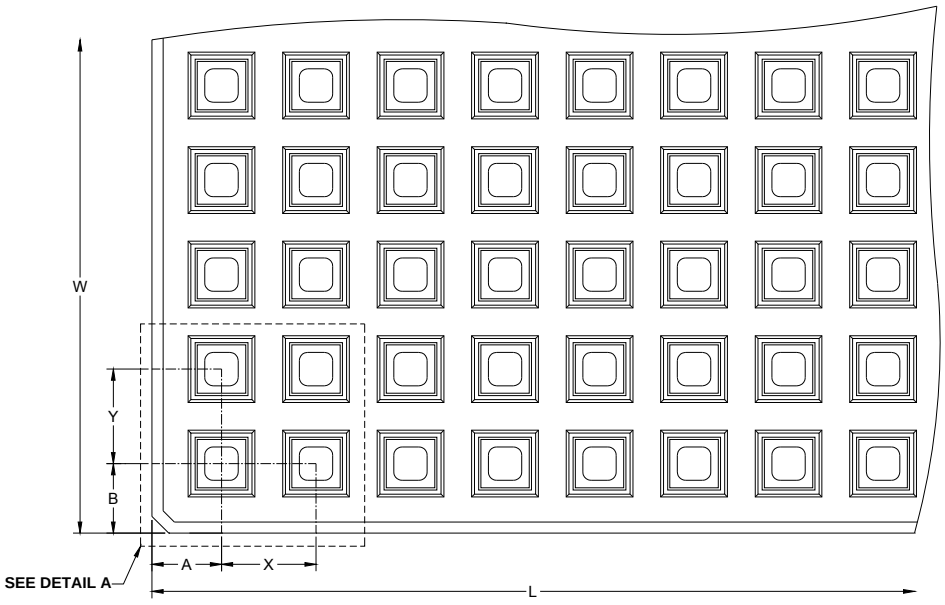
RECOMMENDED LAND PATTERN (Unit: mm)



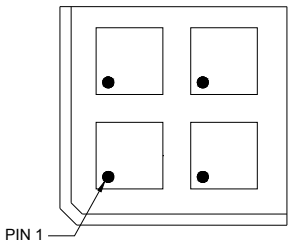
SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32		0.43
c	0.13		0.18
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80 BSC		
L	0.45	0.60	0.75
θ	0°	3.5°	7°

TRAY INFORMATION



TOP VIEW **SIDE VIEW**



DETAIL A

Pin 1 is closest to the chamfered corner of the tray.

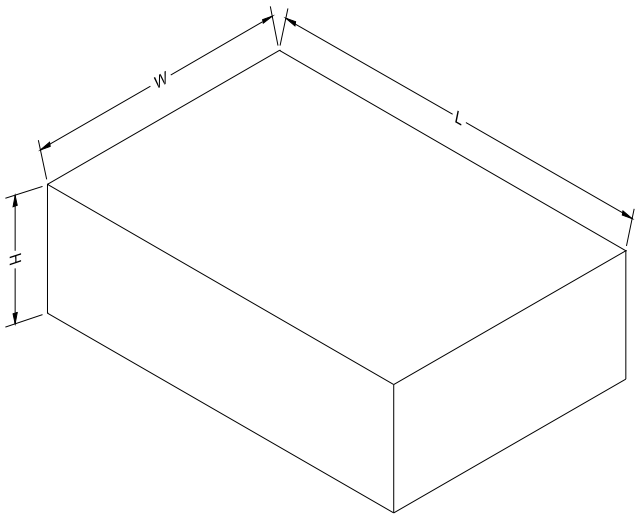
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TRAY

Package Type	A (mm)	B (mm)	X (mm)	Y (mm)	L (mm)	W (mm)	H (mm)	Devices/Tray
LQFP-7×7-32L	11.10	11.25	12.20	12.60	322.6	135.9	7.6	250

DD0003

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Packing Type	Length (mm)	Width (mm)	Height (mm)	Tray/Inner Box	Inner Box/Carton
Tray	560	375	180	2	6

DD0004