# SGM6061
# 55V, 1.5A High Frequency Buck Converter

## GENERAL DESCRIPTION

The SGM6061 is a high voltage and high frequency Buck converter with 1.5A maximum output current and integrated high-side power MOSFET. It implements peak current mode control to simplify external compensation design.

With a wide input voltage range of 3.8V to 55V, it is suitable for a broad range of applications such as industry equipment.

The SGM6061 operates at fixed frequency and enters PFM (Pulse Frequency Modulation) mode automatically at light load to maintain high efficiency. During startup and thermal shutdown, the frequency foldback technique is used to avoid inductor current runaway for reliable and fault tolerant operation. The current limit foldback technique is used for reducing power consumption during output shorted and suppressing output voltage overshot during recovery.

Switching frequency can be set as high as 2MHz. It minimizes the EMI noise issues that could interfere with nearby systems such as AM radio or ADSL modems.

The SGM6061 is available in a Green TDFN-3×3-10L package. It operates over a junction temperature range of -40℃ to +125℃.

## FEATURES

- **Input Voltage Range: 3.8V to 55V**
- **Adjustable Output Range: 0.8V to 24V**
- **Up to 95% Efficiency**
- **PFM Mode at Light Loads**
- **Quiescent Current: 131μA (TYP)**
- **Less than 18μA Shutdown Current**
- **Internal HS Power MOSFET $R_{DSON}$: 250mΩ (TYP)**
- **Adjustable Switching Frequency: up to 2MHz**
- **Adjustable Soft-Start Time**
- **Accurate EN Input Threshold**
- **Stable with Ceramic Capacitor**
- **Available in a Green TDFN-3×3-10L Package**

## APPLICATIONS

Industrial and Commercial Power Systems
Distributed Power Systems
Aftermarket Automotive Accessories

## TYPICAL APPLICATION

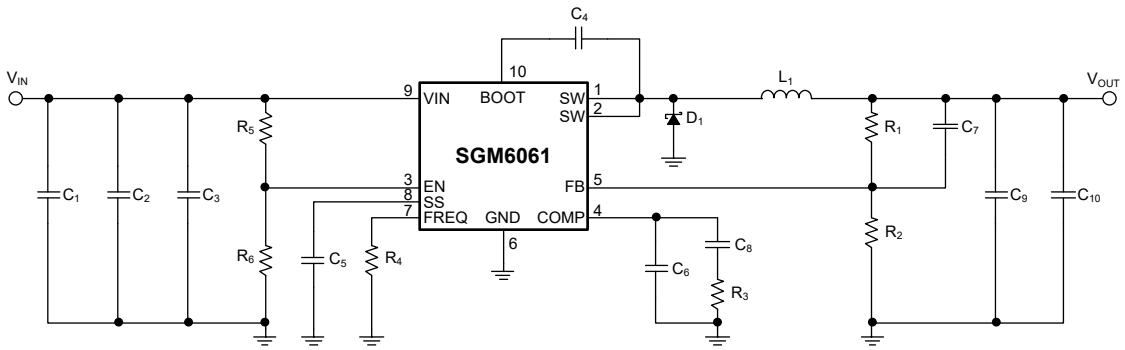


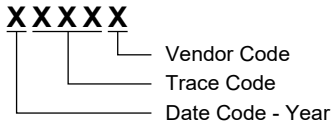

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM6061 | TDFN-3×3-10L | -40℃ to +125℃ | SGM6061XTD10G/TR | SGM<br>6061D<br>XXXXX | Tape and Reel, 4000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, $V_{IN}$ ..... -0.3V to 60V
Switch Voltage Range, $V_{SW}$ .....-0.5V to $V_{IN}$ + 0.5V
BOOT to SW..... -0.3V to 5V
EN Pin Voltage Range, $V_{EN}$ .....-0.3V to $V_{IN}$ + 0.3V
All Other Pins..... -0.3V to 5V
Package Thermal Resistance
TDFN-3×3-10L, $\theta_{JA}$..... 64℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM .....1000V

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, $V_{IN}$ .....3.8V to 55V
Output Voltage Range, $V_{OUT}$.....0.8V to 24V
Operating Junction Temperature Range.....-40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

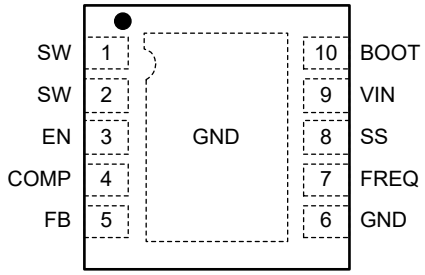
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TDFN-3×3-10L

## PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 2 | SW | Switching Node of the Converter. |
| 3 | EN | Active High Enable Input Pin. It has a weak internal pull-up current source. Pull it below 1.12V to disable the device. Leave EN floating when unused. When EN is directly connected to VIN or external signal source, a resistor greater than 10kΩ is necessary. |
| 4 | COMP | Transconductance Error Amplifier Output. Use a compensation network between COMP and GND pins to compensate the internal loop. |
| 5 | FB | Inverting Input of the Error Amplifier. |
| 6 | GND | Ground Pin. |
| 7 | FREQ | Switching Frequency Adjustment Pin. Connect an external resistor between FREQ and GND pins to adjust the switching frequency. |
| 8 | SS | Soft-Start Time Adjustment Pin. Connect an external capacitor between SS and GND pins to adjust the output ramp-up time. |
| 9 | VIN | Power Supply Input Pin. |
| 10 | BOOT | Power supply of the internal MOSFET gate driver. Connect a 0.1μF bootstrap capacitor between BOOT and SW pins. |
| — | Exposed Pad | Exposed Pad. It should be soldered to the ground plane for enhanced heat dissipation. |

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 12V, $V_{EN}$ = 2V, $T_J$ = +25℃, unless otherwise noted.)

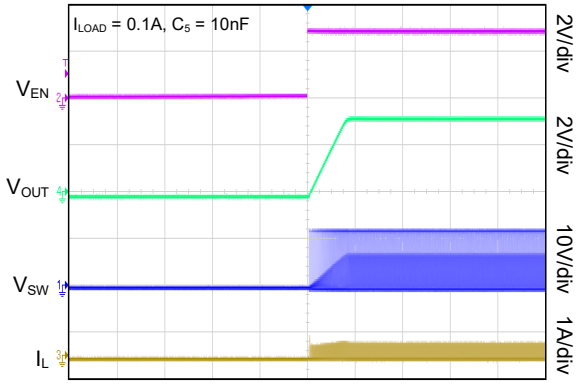
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Feedback Voltage | $V_{FB}$ | $V_{IN}$ = 12V | 0.786 | 0.803 | 0.820 | V |
| | | $T_A$ = -40℃ to +85℃ | 0.784 | | 0.822 | |
| Switch On-Resistance | $R_{DSON}$ | $V_{BOOT}$ - $V_{SW}$ = 5V | | 250 | 315 | mΩ |
| | | $T_A$ = -40℃ to +85℃ | | | 400 | |
| Switch Leakage Current | $I_{LKG}$ | $V_{EN}$ = 0V, $V_{SW}$ = 0V | | 1 | | μA |
| Current Limit | $I_{LIM}$ | | 1.95 | 2.55 | 3.15 | A |
| COMP to Sensed Current Transconductance | $G_{CS}$ | | | 4.5 | | A/V |
| Error Amplifier Voltage Gain (1) | $A_{EA}$ | | | 80 | | dB |
| Error Amplifier Transconductance | $G_{EA}$ | $I_{COMP}$ = ±3μA | | 120 | | μA/V |
| Error Amplifier Source Current | $I_{SOURCE}$ | $V_{FB}$ = 0.7V, $V_{COMP}$ = 1V | | 8.8 | | μA |
| Error Amplifier Sink Current | $I_{SINK}$ | $V_{FB}$ = 0.9V, $V_{COMP}$ = 1V | | -8.6 | | μA |
| VIN Under-Voltage Lockout Threshold (UVLO) | $V_{UVLO}$ | | 2.85 | 3.14 | 3.45 | V |
| | | $T_A$ = -40℃ to +85℃ | 2.7 | | 3.6 | |
| VIN Under-Voltage Lockout Hysteresis | $V_{HYS}$ | | | 0.59 | | V |
| Soft-Start Time (1) | $t_{SS}$ | Timing from EN available, $C_5$ = 10nF | | 1.6 | | ms |
| Soft-Start Current | $I_{SS}$ | $V_{SS}$ = 0V | | 4.9 | | μA |
| Switching Frequency | $f_{SW}$ | $R_4$ = 89kΩ | 0.85 | 1.00 | 1.15 | MHz |
| | | $T_A$ = -40℃ to +85℃ | 0.82 | | 1.16 | |
| Shutdown Supply Current | $I_{SD}$ | $V_{IN}$ = 12V, $V_{EN}$ < 0.2V | | 12.7 | 18 | μA |
| Quiescent Supply Current | $I_Q$ | No Load, $V_{FB}$ = 0.86V | | 131 | | μA |
| Thermal Shutdown Temperature | $T_{SD}$ | Hysteresis = +20℃ | | 155 | | ℃ |
| Minimum Off Time (1) | $t_{OFF\_MIN}$ | | | 100 | | ns |
| Minimum On Time (1) | $t_{ON\_MIN}$ | | | 110 | | ns |
| EN Rising Threshold | $V_{ENR}$ | | 1.40 | 1.58 | 1.75 | V |
| | | $T_A$ = -40℃ to +85℃ | 1.35 | | 1.8 | |
| EN Threshold Hysteresis | $V_{ENHYS}$ | | | 460 | | mV |

NOTE: 1. Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS

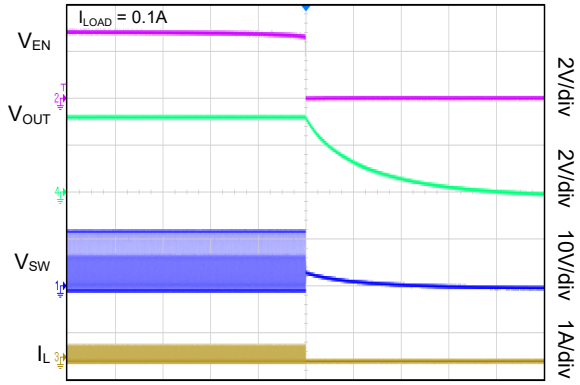
At $T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $C_{IN}$ = 10μF, $C_{OUT}$ = 22μF, $L_1$ = 10μH (DCR = 12mΩ), unless otherwise noted.

Startup



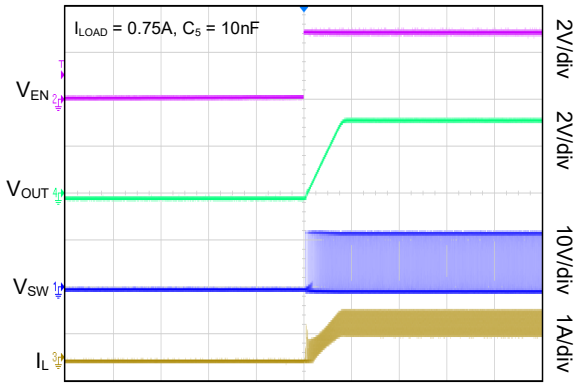

Time (2ms/div)

Shutdown



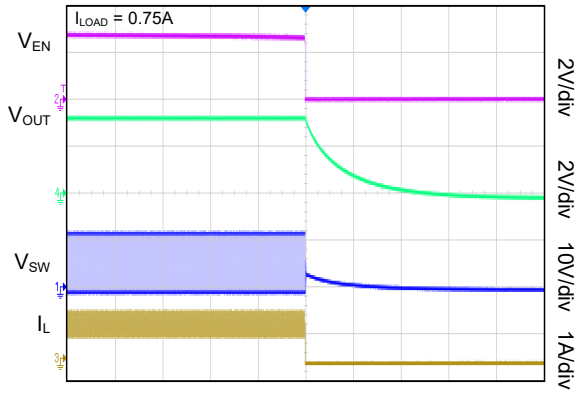

Time (1ms/div)

Startup



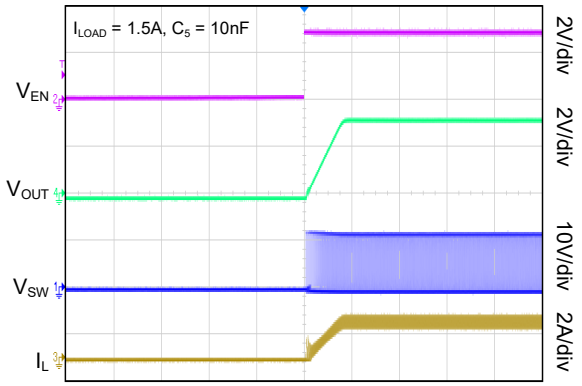

Time (2ms/div)

Shutdown



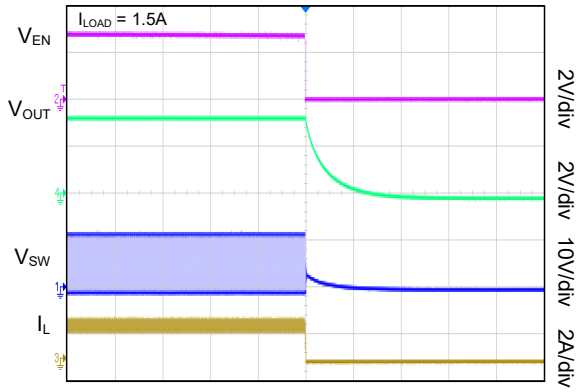

Time (200μs/div)

Startup




Time (2ms/div)

Shutdown

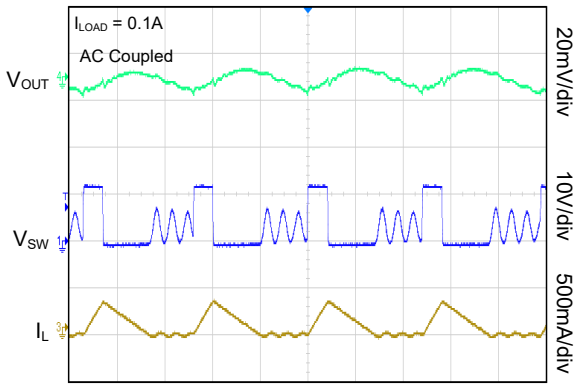



Time (200μs/div)

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

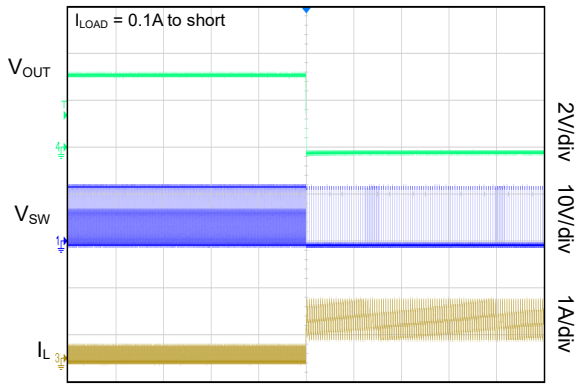
At $T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $C_{IN}$ = 10μF, $C_{OUT}$ = 22μF, $L_1$ = 10μH (DCR = 12mΩ), unless otherwise noted.

Output Ripple



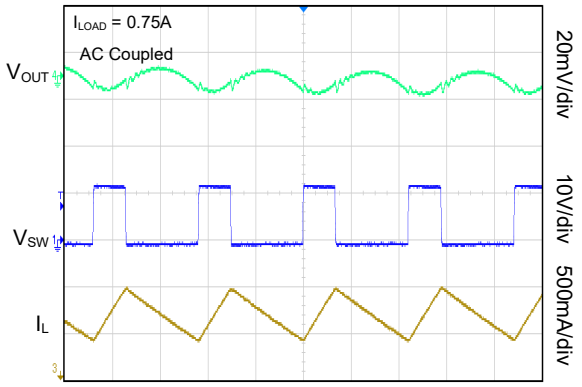

Time (1μs/div)

Short-Circuit Entry



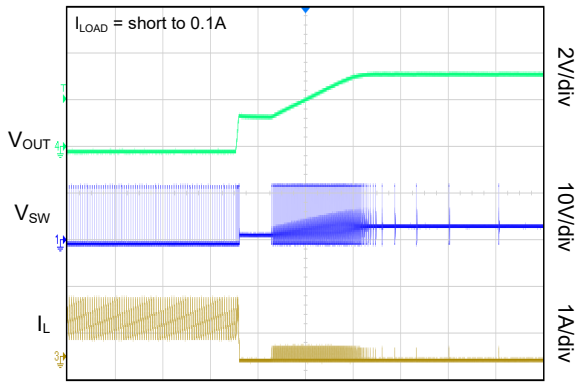

Time (500μs/div)

Output Ripple



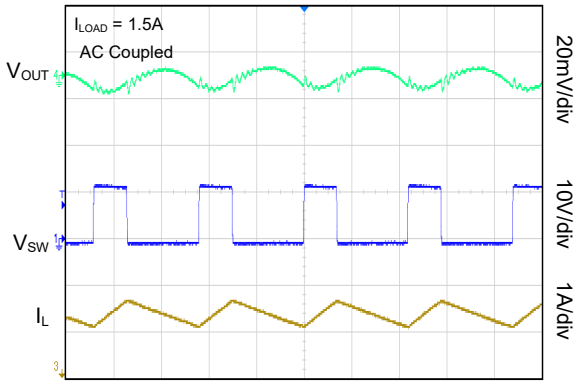

Time (1μs/div)

Short-Circuit Recovery



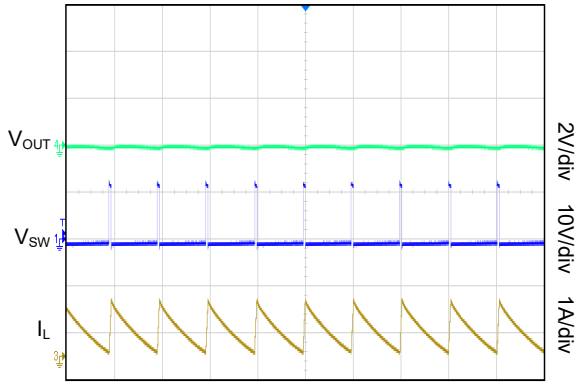

Time (500μs/div)

Output Ripple




Time (1μs/div)

Short-Circuit Steady State

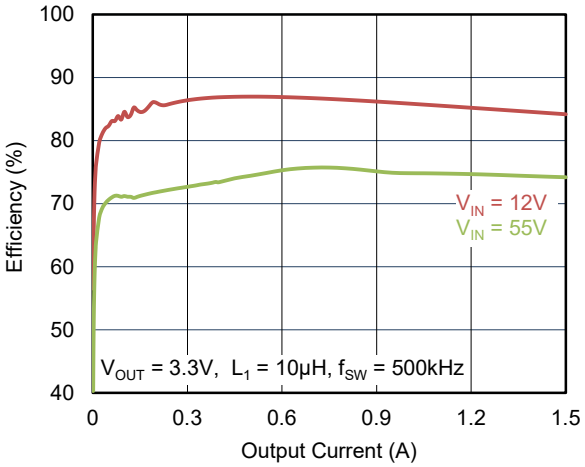



Time (20μs/div)

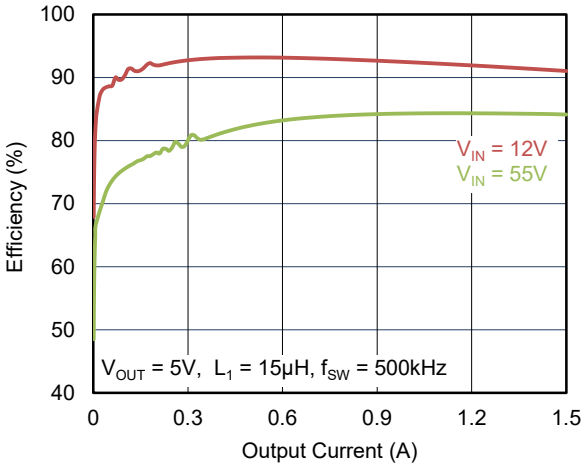
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $C_{IN}$ = 10μF, $C_{OUT}$ = 22μF, $L_1$ = 10μH (DCR = 12mΩ), unless otherwise noted.

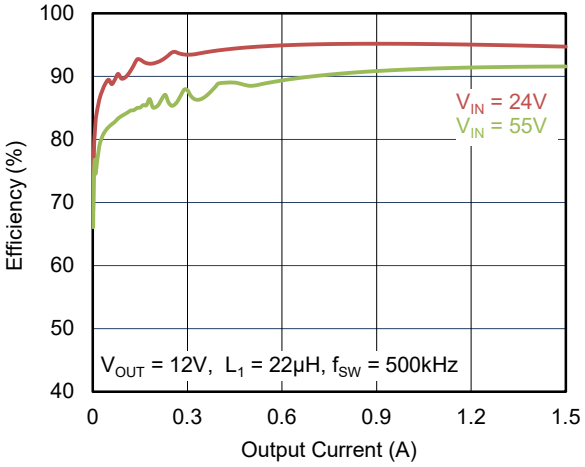
Efficiency vs. Output Current



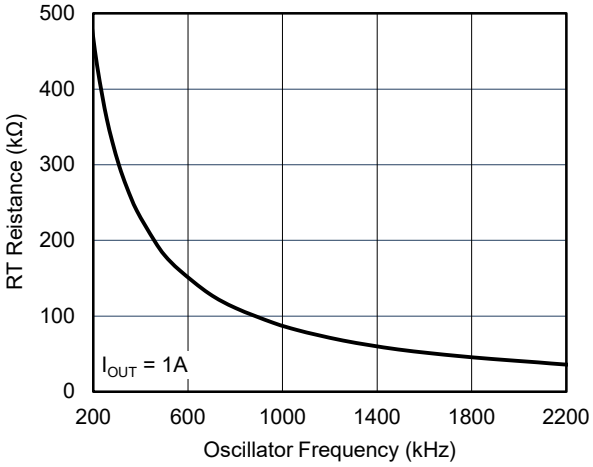

Efficiency vs. Output Current




Efficiency vs. Output Current




RT Resistance vs. Oscillator Frequency



## FUNCTIONAL BLOCK DIAGRAM

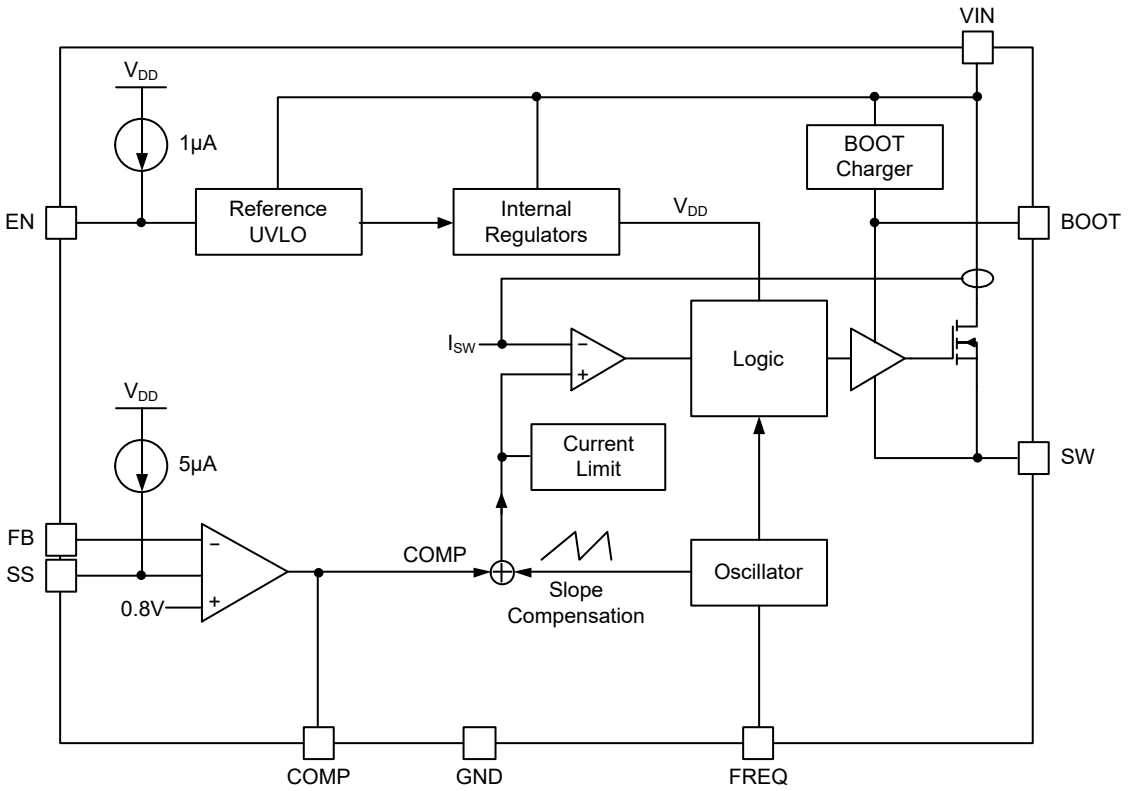



**Figure 2. SGM6061 Functional Block Diagram**

## DETAILED DESCRIPTION

### Overview

The SGM6061 is a 3.8V to 55V, 1.5A non-synchronous Buck converter with integrated high-side N-channel MOSFET. It is a perfect solution for efficient single stage Buck applications. The integrated functions include precision current limiting, automatically switched PWM and PFM modes, adjustable soft-start ramp time and wide range switching frequency, which can meet different requirements. Peak current mode control is implemented to provide fast load transient response and simple compensation.

### VIN Under-Voltage Lockout (UVLO)

The SGM6061 integrates VIN under-voltage lockout (UVLO) feature to protect the device from malfunctioning when the input voltage is insufficient to properly power up the internal circuits. The UVLO rising threshold is 3.14V (TYP) and has a 0.59V (TYP) hysteresis.

### Internal 2.6V Regulator

An internal 2.6V regulator powers most of the device internal circuits. The 2.6V output is fully regulated when $V_{IN}$ exceeds 3.14V. It will drop if $V_{IN}$ falls below 3.14V.

### Enable Input

The EN pin is an active high input to enable or disable the device. The EN rising threshold voltage $V_{ENR}$ is 1.58V (TYP) and has a 460mV (TYP) hysteresis.

A 1μA internal current source pulls the EN pin up to approximately 3.0V. Therefore the device will be enabled when the EN pin is left floating. To disable the device, pull the EN pin down below 1.12V with at least 1μA sink capability.

## DETAILED DESCRIPTION (continued)

When $V_{EN}$ falls below 1.12V, the device is disabled and enters low shutdown current mode. When $V_{EN}$ exceeds 0V and does not reach $V_{ENR}$, the device is still disabled but with slightly higher shutdown current.

### Startup and Shutdown

If both $V_{IN}$ and $V_{EN}$ exceed their thresholds, the device is enabled and starts operation. First, the bandgap circuit starts working to generate stable reference voltage and bias current. Then two internal regulators are established to provide supply voltage for internal analog and digital circuit respectively. About 30μs later, bootstrap capacitor voltage is charged above UVLO threshold. Then SS output starts to rise at the rate set by $C_5$.

The device is disabled when any of invalid EN voltage, VIN UVLO and thermal shutdown events occurs. Once the device is disabled, the high-side switch is turned off immediately to avoid any other fault triggering.

### Soft-Start and Ramp

Every time the device is enabled (after power-up, pulling EN high or a fault recovery), the output voltage is gradually increased to its regulation value with a ramp (after a brief 50μs hold). Soft-start is needed to prevent triggering of current limit or short-circuit protections or to avoid output overshooting during startup. Without a soft-start, the inrush currents of the output capacitors or the load can cause over-current and the protection procedure results in non-monotonic startup or even instability. Overshooting may also occur during startup after short-circuit recovery. The internal soft-start voltage ($V_{SS}$) is almost 0.2V higher than FB voltage ($V_{FB}$). The $V_{SS}$ and reference ($V_{REF}$) are both sent to the error amplifier and the lower value of them is the actual reference that is compared with the feedback voltage ($V_{FB}$).

A 4.9μA pull-up current source is internally connected to the SS pin. The soft-start time ($t_{SS}$) is the time interval that the external soft-start capacitor ($C_5$) voltage increases by 0.8V. Therefore, the soft-start time can be calculated from:

$$t_{ss}(ms) = \frac{C_5(\mu F) \times 0.8V}{I_{SS}} \quad (1)$$

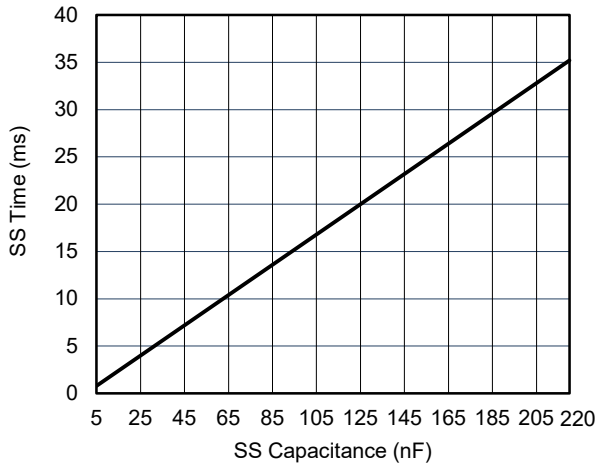



**Figure 3. Recommended SS Time vs. SS Capacitance**

Figure 3 shows the soft-start time with a wide range of external soft-start capacitance values. The recommended soft-start capacitance range is from 5.6nF to 220nF.

### PWM Operation Mode

In the moderate to heavy load conditions, the SGM6061 runs at fixed frequency with peak current control mode. The high-side MOSFET is turned on at the leading edge of internal clock until the sensing current ramp signal reaches the COMP voltage. If the switch current does not reach the reference value (conversion from $V_C$) in a cycle, the switch will also be turned off for $t_{OFF\_MIN}$ (100ns, TYP) before the next clock.

### PFM Mode

In the light load condition, the frequency is reduced depending on the load to minimize the switching and gate driving losses and keep the efficiency high.

### PWM Comparator and Current Limit

For peak current mode, a signal represent of high-side current is used as the input of PWM comparator, which is accurately sampled by internal sensing circuit. After 100ns typical blanking time, the signal is compared with COMP to determine switching state of high-side MOSFET. The cycle-by-cycle current limit threshold is approximately 2.55A.

Note that the measured peak current limits in the closed-loop and open-loop test conditions are slightly different, mainly caused by the propagation delay.

# DETAILED DESCRIPTION (continued)

## Bootstrap Floating MOSFET Driver

The power of the high-side MOSFET driver is provided by an external capacitor between BOOT and SW pins. An internal bootstrap regulator keeps the bootstrap capacitor charged and regulated to approximately 4.5V.

The bootstrap voltage is detected by internal BOOT UVLO circuit with 2.4V rising threshold and 250mV hysteresis. If the bootstrap voltage falls below its UVLO threshold, the power MOSFET is turned off immediately. An internal transistor is used to pull down the SW node to make sure BOOT capacitor is charged sufficiently. This design can obviously reduce the output voltage ripple at small input/output voltage difference and no load. When the bootstrap voltage is charged above threshold, the pull-down transistor is turned off and high-side MOSFET is able to be turned on again.

Except for BOOT UVLO condition, the external circuit connected to the SW serves as the return path to GND for the charge current. Enough voltage headroom should be left to facilitate the charging. When the external freewheeling diode is on, bootstrap charging starts until the regulated voltage.

The converter operates in PFM Mode at no load or light load, to minimize switching losses and keep the output regulated. In this mode, the available time for refreshing the BOOT voltage is reduced, bootstrap voltage will drop below the regulated voltage (4.5V). The maximum charged voltage is equal to $V_{IN}$ - $V_{OUT}$. If the difference of $V_{IN}$ - $V_{OUT}$ is too small, BOOT UVLO can be triggered. The internal charging circuit charges the bootstrap capacitor by the set frequency, until BOOT UVLO is released.

The designer should make sure that the SW node bleeding current is higher than the quiescent current of the floating driver (approximately 20μA). Usually the feedback resistors ($R_1$ and $R_2$) are selected such that the $R_1$ + $R_2$ value is small enough to provide that current:

$$I_{OUT\_MIN} + \frac{V_{OUT}}{(R_1 + R_2)} > 20\mu A \quad (2)$$

## External Bootstrap Diode

To improve the efficiency, using an external boot diode supplied from a 5V rail (in Figure 4) is recommended in the following cases:

- A 5V rail is available.
- $V_{IN}$ is less than 5V.
- $V_{OUT}$ is between 3.3V and 5V.
- High duty cycle applications ($V_{OUT}/V_{IN}$ > 65%).

A low-cost diode like IN4148 or BAT54 can be used.

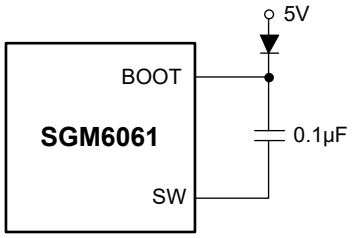



**Figure 4. External Bootstrap Diode**

## Adjustable Switching Frequency

The switching frequency is adjusted by connecting an external resistor ($R_4$) between the FREQ and GND. Use Equation 3 to calculate $R_4$ resistance:

$$R_4(k\Omega) = \frac{94581}{f_{SW}(kHz)} - 7.24 \quad (3)$$

For Example, to get 500kHz switching frequency, the required $R_4$ resistor is 180kΩ.

An internal frequency foldback technique is designed by monitoring the FB voltage. It can effectively avoid the inductor current runaway during startup or restarting in certain situation.

## Error Amplifier (EA)

The output voltage is sensed by a resistor divider through the FB pin and is compared with the internal reference. The EA generates an output current that is proportional to the voltage difference (error). This current is fed into the external compensation network to generate the $V_C$ voltage on the COMP pin, which sets the reference value for the peak current that controls the on time of the power MOSFET.

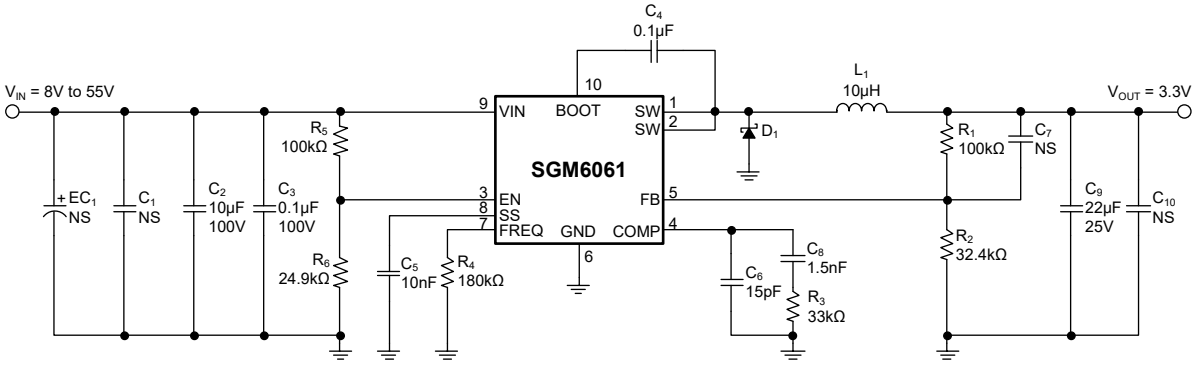
The operating voltage range of COMP ($V_C$) is between 0.75V and 2.0V in normal conditions. COMP is pulled down to the ground when the device shuts down. The COMP voltage must not be pulled higher than 2.6V.

## Thermal Shutdown

To protect the device from damage due to overheating, a thermal shutdown feature is implemented to disable the device when the die temperature exceeds +155℃ (TYP). The chip is automatically enabled when the temperature falls below +135℃ (20℃ hysteresis, TYP).

# APPLICATION INFORMATION

In this section, power supply design with the SGM6061 non-synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.




NOTE: $EC_1$ is optional. If the input voltage is far away from the VIN of SGM6061, $EC_1$ should be installed.

**Figure 5. SGM6061 Application Example with 3.3V/1.5A Output**

## Design Requirements

In this example, a high frequency regulator with ceramic output capacitors will be designed using SGM6061 and the details will be reviewed. The design requirements are typically determined at the system level. The known requirements are summarized in Table 1.

**Table 1. Design Parameters**

| Design Parameter | Example Value |
|---|---|
| Output Voltage | 3.3V |
| Maximum Output Current | 1.5A |
| Load Transient Response of 0.75A - 1.5A Step | $\Delta V_{OUT}$ = 7% |
| Input Voltage Range | 12V nominal, 8V to 55V |
| Maximum Output Voltage Ripple | 33m$V_{P-P}$ |
| Turn-On Input Voltage (Rising $V_{IN}$) | 7.9V |
| Turn-Off Input Voltage (Falling $V_{IN}$) | 5.6V |
| Switching Frequency ($f_{SW}$) | 500kHz |

## Operating Frequency

Usually the first parameter to design is the switching frequency ($f_{SW}$). Higher switching frequencies allow smaller solution size and smaller filter inductors and capacitors, and the bandwidth of the converter can be increased for faster response. It is also easier to filter noises because they also shift to higher frequencies. The drawbacks are increased switching and gate driving losses that result in lower efficiency and tighter thermal limits. Also the duty cycle range and step-down ratio will be limited due to the minimum on-time and/or off-time limits of the converter. In this design, $f_{SW}$ = 500kHz is chosen as a tradeoff. From Equation 3, the nearest standard resistor for this frequency is $R_4$ = 180kΩ.

## Inductor Design

Equation 4 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple ($\Delta I_L$) to the maximum output current ($I_{OUT}$) is represented as $K_{IND}$ factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current ($I_{OUT}$ + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. During power-up with large output capacitor, over-current, output shorted or load transient conditions, the actual peak current of inductor can be greater than $I_{LPEAK}$ calculated in equation 7. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. Typically, a 20% to 40% ripple is selected ($K_{IND}$ = 0.2 ~ 0.4). Choosing a higher $K_{IND}$ value reduces the selected inductance.

$$L_1 = \frac{V_{INMAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (4)$$

## APPLICATION INFORMATION (continued)

In this example, $K_{IND}$ = 0.4 is chosen and the inductance is calculated to be 10.4μH. In this example, the nearest standard value 10μH is selected. The ripple, RMS and peak inductors current calculations are summarized in Equations 5, 6 and 7 respectively.

$$\Delta I_L = \frac{V_{INMAX} - V_{OUT}}{L_1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (5)$$

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (6)$$

$$I_{LPEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

The ripple, RMS, and peak inductor currents are calculated as 0.62A, 1.51A and 1.81A respectively. A 10μH inductor from Sunlord SWPA8040S100MT with 4.1A saturation and 3.3A RMS current ratings is selected.

### External Diode (D)

The SGM6061 adopts non-synchronous architecture. Therefore an external diode is required to place between SW and GND pins. A Schottky diode is recommended due to the characteristics of fast recovery and small forward conduction voltage drop, which can help improve the efficiency and reduce the rising edge ring of SW node.

For main parameters of diode, the maximum reverse voltage rating of the selected diode must be greater than the maximum applicable input voltage. The peak current rating must be greater than the current limit, and the average forward current should be greater than typical load current with enough margin.

In this example, a B380-13-F from Diodes Inc. with 80V reverse voltage and 3A forward current is selected.

### Output Capacitor Design

Three primary criteria must be considered for design of the output capacitor ($C_{OUT}$): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of $V_{OUT}$ in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 8 can be used to calculate the minimum output capacitance that is needed to supply or absorb a current step ($\Delta I_{OUT}$) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of $\Delta V_{OUT}$ (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (8)$$

For example, if the acceptable transient to a 0.75A load step is 7%, by inserting $\Delta V_{OUT}$ = 0.07 × 3.3V = 0.231V and $\Delta I_{OUT}$ = 0.75A, the minimum required capacitance will be 13μF. Generally, the ESR of ceramic capacitors is small enough. The impact of output capacitor ESR on the transient is not taken into account in Equation 8.

Equation 9 can be used for the output ripple criteria and finding the minimum output capacitance needed. $V_{ORIPPLE}$ is the maximum acceptable ripple. In this example, the allowed ripple is 33mV that results in minimum capacitance of 4.7μF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{\Delta I_L}{V_{ORIPPLE}} \quad (9)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 9. Use Equation 10 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement. In this example, the ESR must be less than 33mV/0.62A = 53.2mΩ.

$$R_{ESR} < \frac{V_{ORIPPLE}}{\Delta I_L} \quad (10)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 22μF 25V ceramic capacitor with X7R dielectric and 3mΩ ESR is selected. There is a limit to the amount of ripple current that a capacitor can handle without damage or overheating. The inductor ripple is bypassed through the output capacitor. Equation 11 calculates the RMS current that the output capacitor must support. In this example, it is 179mA.

$$I_{CORMS} = \frac{\Delta I_L}{\sqrt{12}} \quad (11)$$

## APPLICATION INFORMATION (continued)

### Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM6061. If input power is far away from SGM6061, additional bulk capacitor is recommended in parallel to stabilize input voltage. The RMS value of input capacitor can be calculated from Equation 12 and the maximum $I_{CIRMS}$ occurs at 50% duty cycle. For this example, the maximum input RMS current is 0.75A. The ripple current rating of input capacitor should be greater than $I_{CIRMS}$.

$$I_{CIRMS} = I_{OUTMAX} \times \sqrt{D \times (1-D)} \quad (12)$$

where D is the duty cycle.

In this example, the voltage rating of capacitor should have a safe margin from maximum input voltage. Therefore, two 2.2μF/100V ceramic capacitors are selected for VIN to cover all DC bias, thermal and aging deratings, and a 0.1μF/100V capacitor is selected for further decoupling of high frequency noise. The small capacitor should be connected between VIN and GND pins as close as possible.

The input voltage ripple can be calculated from Equation 13, and the maximum ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (13)$$

### Soft-Start Capacitor

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. The ramp is needed in many applications due to limited voltage slew rate required by the load or limited available input current to avoid input voltage sag during startup (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

In this example, the output capacitor value is relatively small and the soft-start time is not critical because it does not require too much charge for 3.3V output voltage. However, it is better to set a small arbitrary value, like $C_5$ = 10nF that results in 1.6ms startup time.

### Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor with 10V or higher voltage rating must be connected between the BOOT and SW pin. X5R or better dielectric types are recommended.

### UVLO Setting

The under-voltage lockout (UVLO) can be programmed by an external voltage divider network. In this design, the turn-on (enable to start switching) occurs when $V_{IN}$ rises above 7.9V ($V_{SATRTUP}$). When the regulator is in operation, it will not stop switching (disabled) until the input falls below 5.6V ($V_{SHUTDOWN}$). Use Equations 13 to calculate the resistors value. In this example, choose $R_5$ = 100kΩ and $R_6$ = 24.9kΩ.

$$R_5 = R_6 \times \frac{V_{STARTUP} - V_{ENR}}{V_{ENR}} \quad (13)$$

### Feedback Resistors

Choosing a 100kΩ value for the upper resistor ($R_1$), the lower resistor ($R_2$) can be calculated from Equation 14. The nearest 1% resistor for the calculated value (32kΩ) is 32.4kΩ. For higher output accuracy, choose resistors with better tolerance (0.5% or better).

$$R_2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_1 \quad (14)$$

### Loop Compensation Design

Several techniques are used by engineers to compensate a DC/DC regulator. In this simplified method, the effects of the slope compensation are ignored. Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

First, the converter pole ($f_P$), and ESR zero ($f_Z$) are calculated from Equations 15 and 16. For $C_{OUT}$, the worst derated value of 20μF should be used. Equations 17 and 18 can be used to find an estimation for closed-loop crossover frequency ($f_{CO}$) as a starting point (choose the lower value).

$$f_P = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (15)$$

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (16)$$

$$f_{CO} = \sqrt{f_P \times f_Z} \quad (17)$$

$$f_{CO} = \sqrt{f_P \times \frac{f_{SW}}{2}} \quad (18)$$

For this design, $f_P$ = 3.62kHz and $f_Z$ = 2.65MHz. Equation 17 yields 98kHz for crossover frequency and Equation 18 gives 30kHz. As the influence of slope compensation in the actual circuit, a slightly higher frequency of 33kHz is selected.

## APPLICATION INFORMATION (continued)

Having the crossover frequency, the compensation network ($R_3$ and $C_8$) can be calculated. $R_3$ sets the gain of the compensated network at the crossover frequency and can be calculated by Equation 19.

$$R_3 = \frac{2\pi \times f_{CO} \times V_{OUT} \times C_{OUT}}{G_{EA} \times V_{REF} \times G_{CS}} \quad (19)$$

$C_8$ sets the location of the compensation zero along with $R_3$. To place this zero on the converter pole, use Equation 20.

$$C_8 = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_3} \quad (20)$$

From Equations 19 and 20, the standard selected values are $R_3$ = 33kΩ and $C_8$ = 1.5nF.

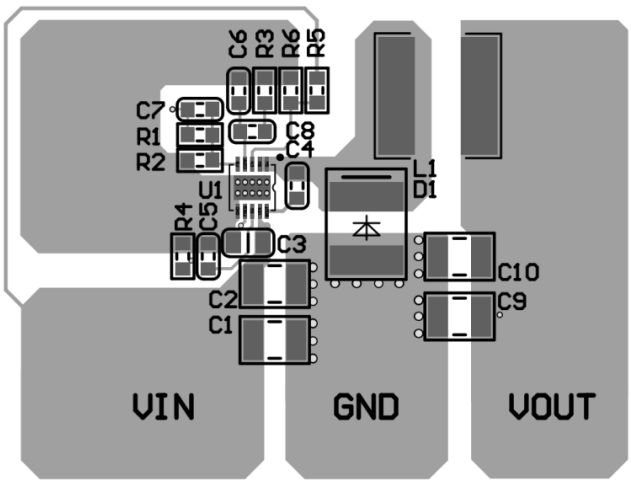
A high frequency pole can also be added by a parallel capacitor if needed (not used in this example). The pole frequency can be calculated from Equation 21.

$$f_P = \frac{I_{OUT}}{2\pi \times R_3 \times C_6} \quad (21)$$

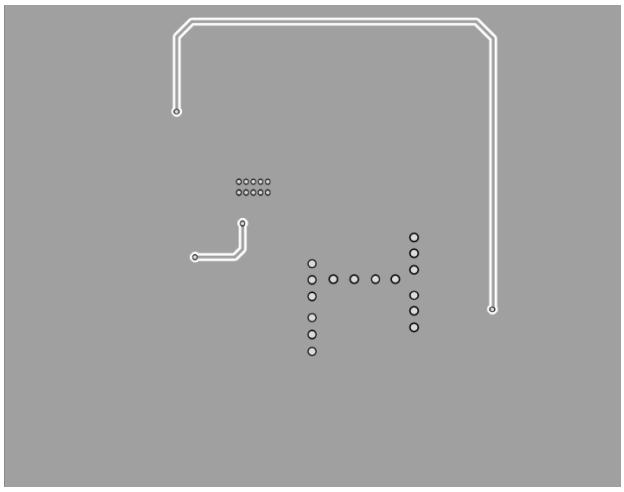
### Layout Considerations

PCB layout is critical for stable and high-performance converter operation. The recommend layout is shown in Figure 6.

- Place the nearest input high frequency decoupling capacitor (0.1μF) between VIN and GND pins as close as possible.
- Place the larger input ceramic capacitor and Schottky diode close to relevant pins for minimizing the influence of ground bounce.
- Use short and wide trace to connect SW node to the inductor. Minimize the area of switching loop. Otherwise, large voltage spikes on the SW node and poor EMI performance are inevitable.
- Sensitive signal like FB, COMP, EN traces must be placed away from high dv/dt nodes (such as SW) and not inside any high di/dt loop (like capacitor or switch loops). The ground of these signals should be connected to GND pin and separated with power ground.
- To improve the thermal relief, use a group of thermal vias under the exposed pad to transfer the heat to the ground planes in the opposite side of the PCB. Use small vias (approximately 15mil) such that they can be filled up during the reflow soldering process to provide a good metallic heat conduction path from the IC exposed pad to the other PCB side.
- Connect VIN, GND and exposed pad pins to large copper areas to increase heat dissipation and long-term reliability. Keep SW area small to avoid emission issue.




Top Layer



Bottom Layer

**Figure 6. PCB Layout Guide**

# ADDITIONAL TYPICAL APPLICATION CIRCUITS

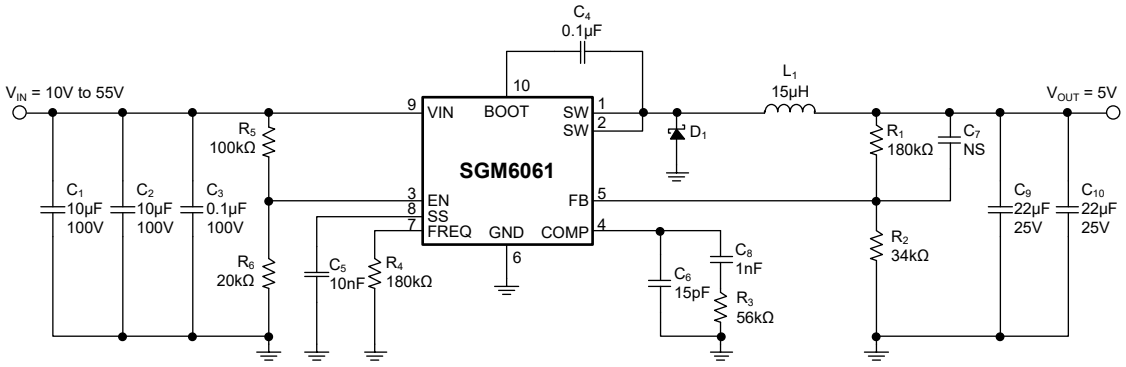



**Figure 7. 5V Output Typical Application (NS: not soldered)**

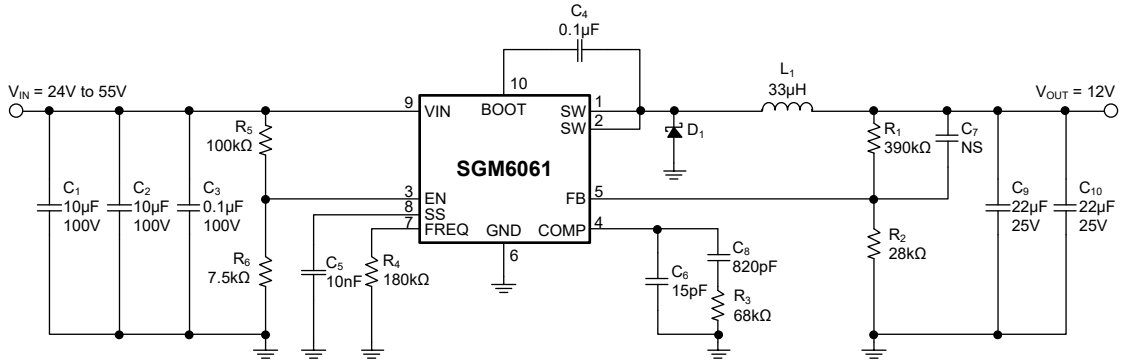



**Figure 8. 12V Output Typical Application (NS: not soldered)**

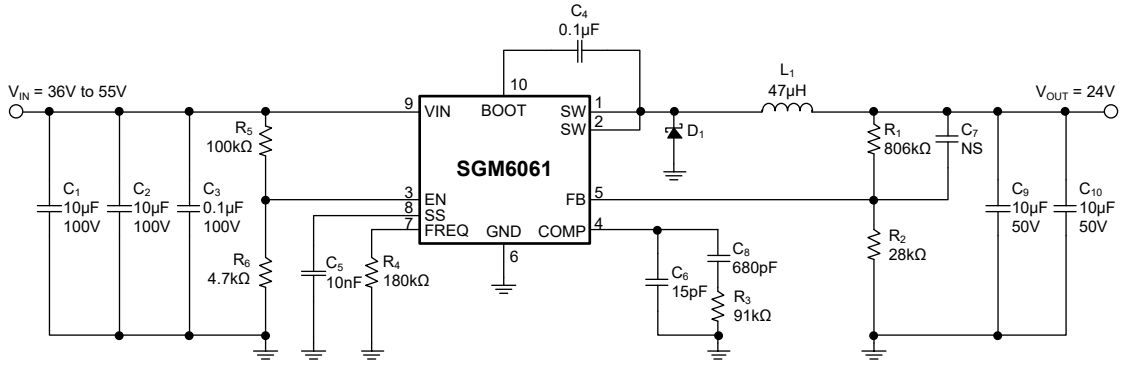



**Figure 9. 24V Output Typical Application (NS: not soldered)**

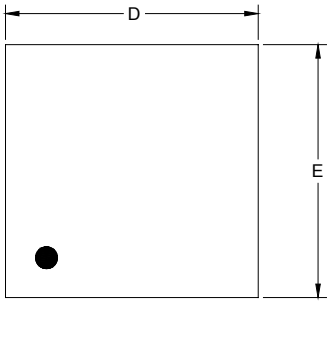
# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

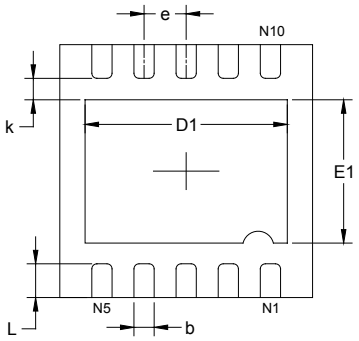
| Changes from Original (MARCH 2022) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

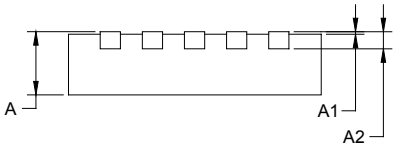
## TDFN-3×3-10L



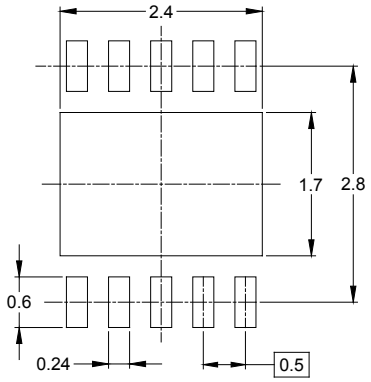

TOP VIEW




BOTTOM VIEW




SIDE VIEW

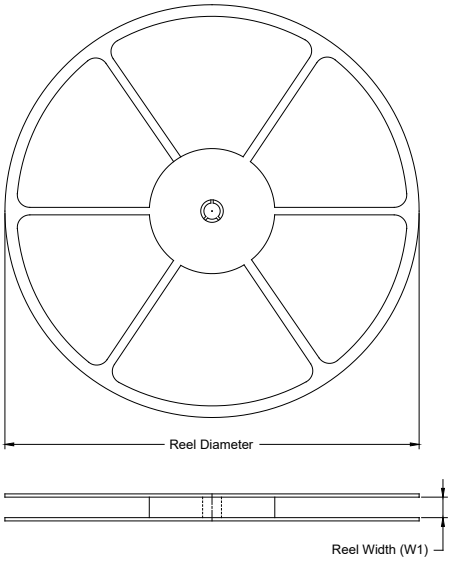



**RECOMMENDED LAND PATTERN** (Unit: mm)

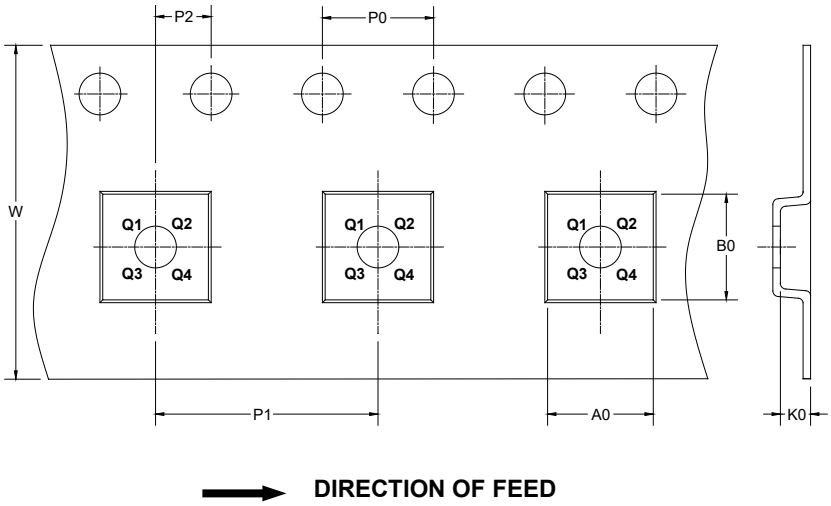
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A2 | 0.203 REF | | 0.008 REF | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.300 | 2.600 | 0.091 | 0.103 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 1.500 | 1.800 | 0.059 | 0.071 |
| k | 0.200 MIN | | 0.008 MIN | |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| e | 0.500 TYP | | 0.020 TYP | |
| L | 0.300 | 0.500 | 0.012 | 0.020 |

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



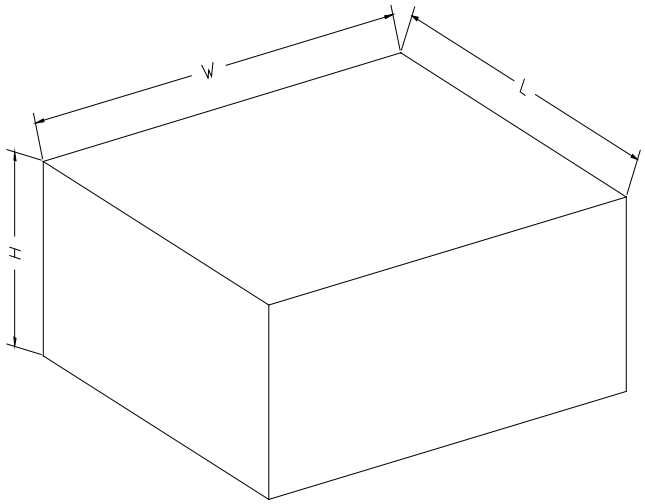

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TDFN-3×3-10L | 13″ | 12.4 | 3.35 | 3.35 | 1.13 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002