74LVTN16245 3.3V, 16-Bit Transceiver with Direction Pin and 3-State Outputs

GENERAL DESCRIPTION

The 74LVTN16245 is a high-performance 16-bit transceiver for 3.3V V_{CC} operation, but with the capability to provide an interface to 5V system environment. The non-inverting 3-state bus compatible outputs are available in both sending and receiving directions.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. The direction control (nDIR) input determines the direction of the data flow. nDIR (active high) enables data from nAn port to nBn port. nDIR (active low) enables data from nBn port to An port. The output enable (\overline{nOE}) input, when high, disables both nAn and nBn ports by placing them in a high-impedance state.

FEATURES

- Wide Operating Voltage Range: 2.7V to 3.6V
- Input and Output Interface Capability to 5V System Environment
- +64mA/-32mA Output Current
- 3-State Outputs Drive Bus Lines Directly
- Power-up and I_{OFF} 3-State
- -40°C to +125°C Operating Temperature Range
- Available in a Green TSSOP-48 Package

FUNCTION TABLE

CONTRO	L INPUT	INPUT/OUTPUT			
nŌĒ	nDIR	nAn	nBn		
L	L	nAn = nBn	Inputs		
L	Н	Inputs	nBn = nAn		
Н	X	Z	Z		

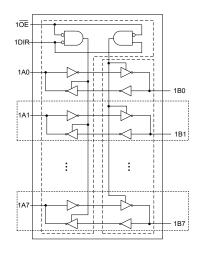
H = High Voltage Level

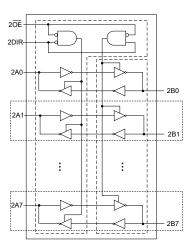
L = Low Voltage Level

Z = High-Impedance State

X = Don't Care

LOGIC DIAGRAM



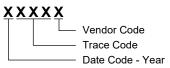


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVTN16245	TSSOP-48	-40°C to +125°C	74LVTN16245XTS48G/TR	74LVTN16245 XTS48 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V _{CC} Input Voltage, V _I ⁽²⁾	
Output Voltage, V _O ⁽²⁾	
Output in 3-State or High-State	0.5V to 7V
Input Clamping Current, I _{IK} (V _I < 0V)	50mA
Output Clamping Current, $I_{OK}(V_O < 0V)$	50mA
Output Current, I _O	
Output in High-State	64mA
Output in Low-State	128mA
Supply Current, I _{CC}	128mA
Ground Current, I _{GND}	
Junction Temperature (3)	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	8000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V _{CC}	2.7V to 3.6V
Input Voltage, V _I	0V to 5.5V
High-Level Output Current, I _{OH}	32mA
Low-Level Output Current, IoL	64mA
Input Transition Rise and Fall Rate, $\Delta t/\Delta l$	V
	10ns/V (MAX)
Operating Temperature Range	40°C to +125°C

OVERSTRESS CAUTION

- 1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.
- 2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

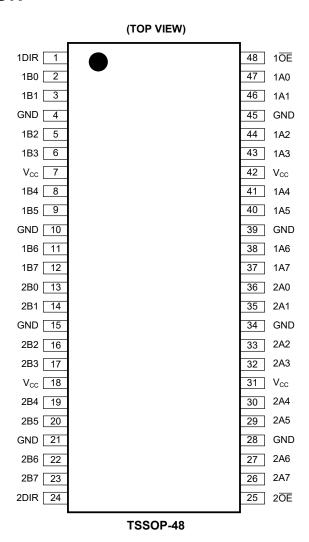
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 24	1DIR, 2DIR	Direction Control.
2, 3, 5, 6, 8, 9, 11, 12	1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	Data Inputs/Outputs.
13, 14, 16, 17, 19, 20, 22, 23	2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	Data Inputs/Outputs.
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground.
7, 18, 31, 42	V _{CC}	Supply Voltage.
48, 25	1 OE , 2 OE	Output Enable Inputs (Active Low).
36, 35, 33, 32, 30, 29, 27, 26	2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	Data Inputs/Outputs.
47, 46, 44, 43, 41, 40, 38, 37	1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	Data Inputs/Outputs.

ELECTRICAL CHARACTERISTICS

(Full = -40°C to +125°C, all typical values are measured at V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDI	TIONS	TEMP	MIN	TYP	MAX	UNITS
Input Clamping Voltage	V _{IK}	$V_{CC} = 2.7V, I_{IK} = -18mA$	V _{CC} = 2.7V, I _{IK} = -18mA			-0.78		V
High-Level Input Voltage	V _{IH}	V _{CC} = 2.7V to 3.6V		Full	2.0			V
Low-Level Input Voltage	V _{IL}	V _{CC} = 2.7V to 3.6V		Full			0.8	V
		V_{CC} = 2.7V to 3.6V, I_{OH} =	-100µA	Full	V _{CC} - 0.05	V _{CC} - 0.001		
High-Level Output Voltage	V _{OH}	V _{CC} = 2.7V, I _{OH} = -8mA		Full	2.45	2.60		V
		V _{CC} = 3.0V, I _{OH} = -32mA		Full	2.10	2.65		
		V 0.7V	I _{OL} = 100μA	Full		0.001	0.05	
		V _{CC} = 2.7V	I _{OL} = 24mA	Full		0.15	0.28	
Low-Level Output Voltage	V _{OL}		I _{OL} = 16mA	Full		0.1	0.18	V
		V _{CC} = 3.0V	I _{OL} = 32mA	Full		0.2	0.36	
			I _{OL} = 64mA	Full		0.4	0.55	
		Control pins, $V_{CC} = 3.6V$, $V_I = V_{CC}$ or GND		Full		±0.01	±1	
	I ₁	Control pins, V _{CC} = 0V or 3.6V, V _I = 5.5V		Full		0.01	5	μΑ
Input Leakage Current		Input/output data pins ⁽¹⁾ , V _{CC} = 3.6V, V _I = 5.5V		Full		1	5	
		Input/output data pins $^{(1)}$, $V_{CC} = 3.6V$, $V_{I} = V_{CC}$		Full		0.01	1	
		Input/output data pins ⁽¹⁾ , V _{CC} = 3.6V, V _I = 0V		Full	-2	-0.01		
Output Leakage Current	I _{LO}	Output in high-state whe $V_O = 5.5V$, $V_{CC} = 3.0V$		Full		1	30	μΑ
Power-Up/Down Output Current	I _{O_PU/PD}	$V_{CC} \le 1.2V$, $V_O = 0.5V$ to V $n\overline{OE} = don't care$	V_{CC} , $V_I = GND$ or V_{CC} ,	+25°C		0.01	10	μA
Power-Off Leakage Current	I _{OFF}	$V_{CC} = 0V$, V_I or $V_O = 0V$ t	o 5.5V	Full		0.01	10	μA
		V _{CC} = 3.6V,	Output high	Full		16	90	
Supply Current	I _{cc}	$V_1 = GND \text{ or } V_{CC}$	Output low	Full		16	90	μΑ
		I _O = 0A	Outputs disabled (2)	Full		16	85	1
Additional Supply Current	ΔI_{CC}	Per input pin, V_{CC} = 3.0V to 3.6V, one input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		Full		0.2	80	μΑ
Input Capacitance	Cı	DIR and $n\overline{OE}$ inputs, V_I		+25°C		6		pF
Input/Output Capacitance	C _{I/O}	At input/output data pins $V_{I/O} = 0V$ or 3.0V	, outputs disabled,	+25°C		9		pF

NOTES

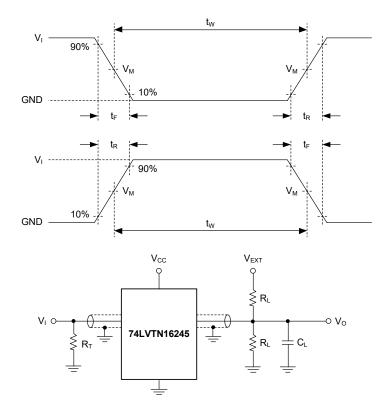
- 1. Other pins must be tied to $\ensuremath{V_{\text{CC}}}$ or GND and should not be floating.
- 2. I_{CC} is measured with outputs pulled to V_{CC} or GND.

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. All typical values are measured at Vcc = 3.3V and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIO	NS	TEMP	MIN	TYP	MAX	UNITS
Low to High Propagation Dolov	+	nAn to nBn or nBn to nAn,	V _{CC} = 2.7V	+25°C		4.3		no
Low to High Propagation Delay	t _{PLH}	See Figure 2	V _{CC} = 3.0V to 3.6V	+25°C		4.3		ns
High to Low Propagation Doloy	+	nAn to nBn or nBn to nAn,	V _{CC} = 2.7V	+25°C		3.9		20
High to Low Propagation Delay	t _{PHL}	See Figure 2	V _{CC} = 3.0V to 3.6V	+25°C		3.7		ns
Off State to High Propagation Poley	Inzu	nOE to nAn or nBn,	V _{CC} = 2.7V	+25°C		5.3		no
Off-State to High Propagation Delay		See Figure 3	V _{CC} = 3.0V to 3.6V	+25°C		4.9		ns
Off State to Law Propagation Delay	t _{PZL}	nOE to nAn or nBn,	V _{CC} = 2.7V	+25°C		5		- ns
Off-State to Low Propagation Delay		See Figure 3	V _{CC} = 3.0V to 3.6V	+25°C		4.9		
Lighto Off State Propagation Policy	4	nOE to nAn or nBn,	V _{CC} = 2.7V	+25°C		4.9		20
High to Off-State Propagation Delay	t _{PHZ}	See Figure 3	V _{CC} = 3.0V to 3.6V	+25°C		4.6		ns
Louise Off State Propagation Delay		nOE to nAn or nBn,	V _{CC} = 2.7V	+25°C		5.4		ns
Low to Off-State Propagation Delay	t_{PLZ}	See Figure 3	V _{CC} = 3.0V to 3.6V	+25°C		5.4		

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

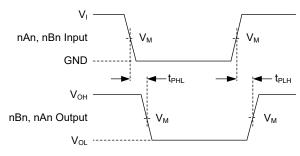
V_{EXT}: External voltage used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	IN	PUT	LO	AD	V _{EXT}		
V _{CC}	Vı	t _R , t _F	C∟	R _L	t _{PHZ} , t _{PZH} t _{PLZ} , t _{PZL}		t _{PLH} , t _{PHL}
2.7V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	GND	6V	Open

WAVEFORMS

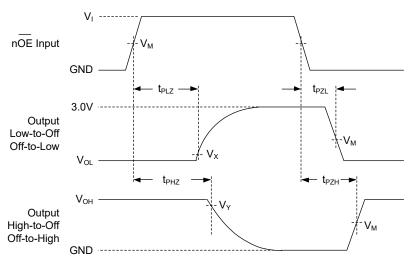


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nAn, nBn) to Output (nBn, nAn) Propagation Delays



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INP	TUT	OUTPUT			
V _{cc}	Vı	V _M ⁽¹⁾	V _M	V _Y		
2.7V to 3.6V	2.7V	1.5V	1.5V	V _{OL} + 0.3V	V _{OH} - 0.3V	

NOTE: 1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

3.3V, 16-Bit Transceiver with Direction Pin and 3-State Outputs

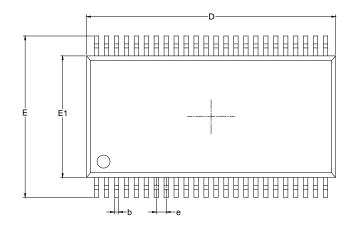
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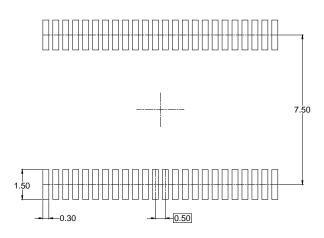
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

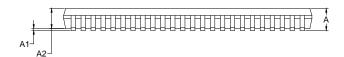
JANUARY 2022 – REV.A to REV.A.1	Page
Updated I _I and I _{CC} values in Electrical Characteristics section	4
Changes from Original (MARCH 2021) to REV.A	Page
Changed from product preview to production data	All

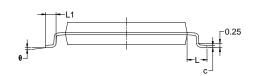
PACKAGE OUTLINE DIMENSIONS TSSOP-48





RECOMMENDED LAND PATTERN (Unit: mm)





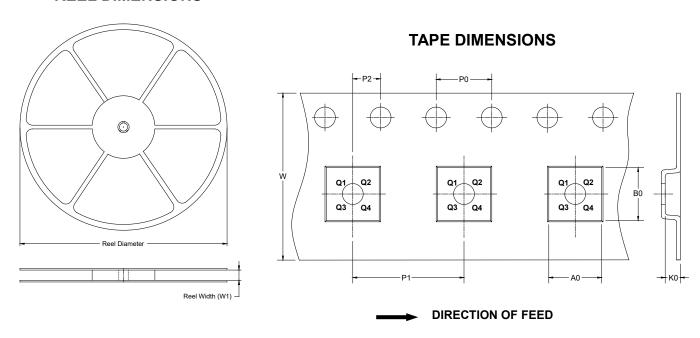
Cymphal	Di	Dimensions In Millimeters						
Symbol	MIN	MOD	MAX					
Α			1.20					
A1	0.05	0.10	0.15					
A2	0.85	0.95	1.05					
b	0.18		0.26					
С	0.15		0.19					
D	12.40	12.50	12.60					
Е	7.90	8.10	8.30					
E1	6.00	6.10	6.20					
е		0.50 BSC						
L		1.00 REF						
L1	0.45		0.75					
θ	0°		8°					

- NOTES:

 1. Body dimensions do not include mode flash or protrusion.
- 2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



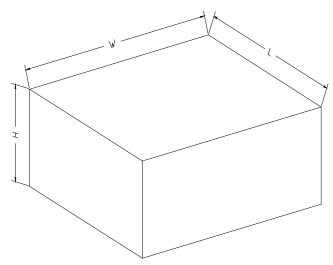
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-48	13"	24.4	8.60	13.00	1.80	4.0	12.0	2.0	24.0	Q1

TX10000.000

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5