

## JEITA Compliant Stand-Alone Switch-Mode Li-Ion and Li-Polymer Battery Charger with Integrated MOSFETs and Power Path Selector

Check for Samples: [bq24171](#)

### FEATURES

- JEITA Compatible Battery Temperature Sensing
- 1.6MHz Synchronous Switch-Mode Charger with 4A Integrated N-MOSFETs
- Up to 94% Efficiency
- 30V Input Rating with Adjustable Over-Voltage Protection
  - 4.5V to 17V Input Operating Voltage
- Battery Charge Voltage
  - 1, 2, or 3-Cell with 4.2V/Cell
- High Integration
  - Automatic Power Path Selector Between Adapter and Battery
  - Dynamic Power Management
  - Integrated 20-V Switching MOSFETs
  - Integrated Bootstrap Diode
  - Internal Loop Compensation
  - Internal Digital Soft Start
- Safety
  - Thermal Regulation Loop Throttles Back Current to Limit  $T_j = 120^{\circ}\text{C}$
  - Thermal Shutdown
  - Battery Thermistor Sense Hot/Cold Charge Suspend & Battery Detect
  - Input Over-Voltage Protection with Programmable Threshold
  - Cycle-by-Cycle Current Limit
- Accuracy
  - $\pm 0.5\%$  Charge Voltage Regulation
  - $\pm 4\%$  Charge Current Regulation
  - $\pm 4\%$  Input Current Regulation
- Less than 15 $\mu\text{A}$  Battery Current with Adapter Removed
- Less than 1.5mA Input Current with Adapter Present and Charge Disabled
- Small QFN Package
  - 3.5mm  $\times$  5.5mm QFN-24 Pin

### APPLICATIONS

- Tablet PC
- Netbook and Ultra-Mobile Computers
- Portable Data Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Back-Up Systems

### DESCRIPTION

The bq24171 is highly integrated stand-alone Li-ion and Li-polymer switch-mode battery charger with two integrated N-channel power MOSFETs. It offers a constant-frequency synchronous PWM controller with high accuracy regulation of input current, charge current, and voltage. It closely monitors the battery pack temperature and allows charge only in a JEITA profile compatible window with lower charge rate at low temperature and lower charge voltage at high temperature. It also provides battery detection, pre-conditioning, charge termination, and charge status monitoring. The thermal regulation loop reduces charge current to maintain the junction temperature of 120°C during operation.

The bq24171 charges the battery in three phases: preconditioning, constant current, and constant voltage. It is adjustable for up to three series Li+ cells.

Charge is terminated when the current reaches 10% of the fast charge rate. A programmable charge timer offers a safety back up. The bq24171 automatically restarts the charge cycle if the battery voltage falls below an internal threshold, and enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage.

The bq24171 features Dynamic Power Management (DPM) to reduce the charge current when the input power limit is reached to avoid over-loading the adapter. A highly-accurate current-sense amplifier enables precise measurement of input current from adapter to monitor overall system power.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

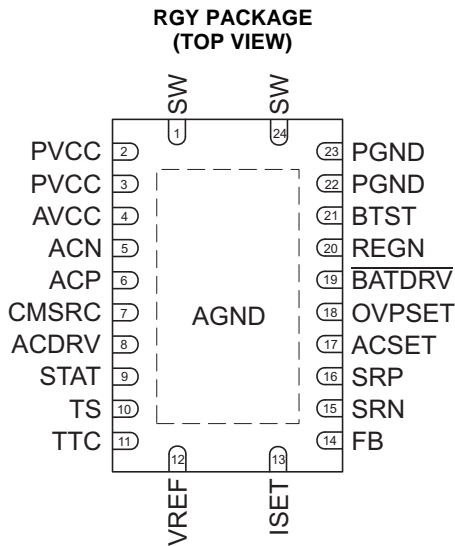
DESCRIPTION (CONTINUED)

The bq24171 provides power path selector gate driver ACDRV/CMSRC on input NMOS pair ACFET (Q1) and RBFET (Q2), and BATDRV on a battery PMOS device (Q3). When the qualified adapter is present, the system is directly connected to the adapter. Otherwise, the system is connected to the battery. In addition, the power path prevents battery from boosting back to the input.

The bq24171 charges battery from DC source as high as 17V, including car battery. The input over-voltage limit is adjustable through OVPSET pin. The AVCC, ACP and ACN pins are 30V rating. When a high-voltage DC source is inserted, Q1/Q2 remain off to avoid high-voltage damage to the system.

For 1 cell applications, if the battery is not removable, the system can be directly connected to the battery to simplify the power path design and lower the cost. With this configuration, the battery can automatically supplement the system load if the adapter is overloaded.

The bq24171 is available in a 24-pin, 3.5mmx5.5 mm thin QFN package.



PIN FUNCTIONS

| PIN  |       | TYPE | DESCRIPTION  |
|------|-------|------|--|
| NO.  | NAME  |      |  |
| 1,24 | SW    | P    | Switching node, charge current output inductor connection. Connect the 0.047-μF bootstrap capacitor from SW to BTST.   |
| 2,3  | PVCC  | P    | Charger input voltage. Connect at least 10-μF ceramic capacitor from PVCC to PGND and place it as close as possible to IC.   |
| 4    | AVCC  | P    | IC power positive supply. Place a 1-μF ceramic capacitor from AVCC to AGND and place it as close as possible to IC. Place a 10-Ω resistor from input side to AVCC pin to filter the noise. For 5V input, a 5-Ω resistor is recommended.                      |
| 5    | ACN   | I    | Adapter current sense resistor negative input. A 0.1-μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering.                   |
| 6    | ACP   | P/I  | Adapter current sense resistor positive input. A 0.1-μF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering.                             |
| 7    | CMSRC | O    | Connect to common source of N-channel ACFET and reverse blocking MOSFET (RBFET). Place 4-kΩ resistor from CMSRC pin to the common source of ACFET and RBFET to control the turn-on speed. The resistance between ACDRV and CMSRC should be 500-kΩ or bigger. |

## PIN FUNCTIONS (continued)

| PIN         |        | TYPE | DESCRIPTION  |
|-------------|--------|------|--|
| NO.         | NAME   |      |  |
| 8           | ACDRV  | O    | AC adapter to system switch driver output. Connect to 4-kΩ resistor then to the gate of the ACFET N-channel power MOSFET and the reverse conduction blocking N-channel power MOSFET. Connect both FETs as common-source. The internal gate drive is asymmetrical, allowing a quick turn-off and slower turn-on in addition to the internal break-before-make logic with respect to the BATDRV.                                 |
| 9           | STAT   | O    | Open-drain charge status pin with 10-kΩ pull up to power rail. The STAT pin can be used to drive LED or communicate with the host processor. It indicates various charger operations: LOW when charge in progress. HIGH when charge is complete or in SLEEP mode. Blinking at 0.5Hz when fault occurs, including charge suspend, input over-voltage, timer fault and battery absent.   |
| 10          | TS     | I    | Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to AGND. The 103AT thermistor is recommended.  |
| 11          | TTC    | I    | Safety Timer and termination control. Connect a capacitor from this node to AGND to set the fast charge safety timer(5.6min/nF). Pre-charge timer is internally fixed to 30 minutes. Pull the TTC to LOW to disable the charge termination and safety timer. Pull the TTC to HIGH to disable the safety timer but allow the charge termination.  |
| 12          | VREF   | P    | 3.3V reference voltage output. Place a 1-μF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for programming ISET and ACSET and TS pins.  |
| 13          | ISET   | I    | Fast charge current set point. Use a voltage divider from VREF to ISET to AGND to set the fast charge current:<br>$I_{CHG} = \frac{V_{ISET}}{20 \times R_{SR}}$<br>The pre-charge and termination current is internally as one tenth of the charge current. The charger is disabled when ISET pin voltage is below 40mV and enabled when ISET pin voltage is above 120mV.  |
| 14          | FB     | I    | Charge voltage analog feedback adjustment. Connect the output of a resistor divider powered from the battery terminals to FB to AGND. Output voltage is regulated to 2.1V on FB pin during constant-voltage mode.  |
| 15          | SRN    | I    | Charge current sense resistor negative input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from SRN pin to AGND for common-mode filtering.  |
| 16          | SRP    | I/P  | Charge current sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from SRP pin to AGND for common-mode filtering.   |
| 17          | ACSET  | I    | Input current set point. Use a voltage divider from VREF to ACSET to AGND to set this value:<br>$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}}$   |
| 18          | OVPSET | I    | Valid input voltage set point. Use a voltage divider from input to OVPSET to AGND to set this voltage. The voltage above internal 1.6V reference indicates input over-voltage, and the voltage below internal 0.5V reference indicates input under-voltage. In either condition, charge terminates, and input NMOS pair ACFET/RBFET turn off. LED driven by STAT pin keeps blinking, reporting fault condition.                |
| 19          | BATDRV | O    | Battery discharge MOSFET gate driver output. Connect to 1kohm resistor to the gate of the BATFET P-channel power MOSFET. Connect the source of the BATFET to the system load voltage node. Connect the drain of the BATFET to the battery pack positive node. The internal gate drive is asymmetrical to allow a quick turn-off and slower turn-on, in addition to the internal break-before-make logic with respect to ACDRV. |
| 20          | REGN   | P    | PWM low side driver positive 6V supply output. Connect a 1-μF ceramic capacitor from REGN to PGND pin, close to the IC. Generate high-side driver bootstrap voltage by integrated diode from REGN to BTST.   |
| 21          | BTST   | P    | PWM high side driver positive supply. Connect the 0.047-μF bootstrap capacitor from SW to BTST.  |
| 22,23       | PGND   | P    | Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. Only connect to AGND through the Thermal Pad underneath the IC.   |
| Thermal Pad | AGND   | P    | Exposed pad beneath the IC. Always solder Thermal Pad to the board, and have vias on the Thermal Pad plane star-connecting to AGND and ground plane for high-current power converter. It dissipates the heat from the IC.  |

## TYPICAL APPLICATIONS

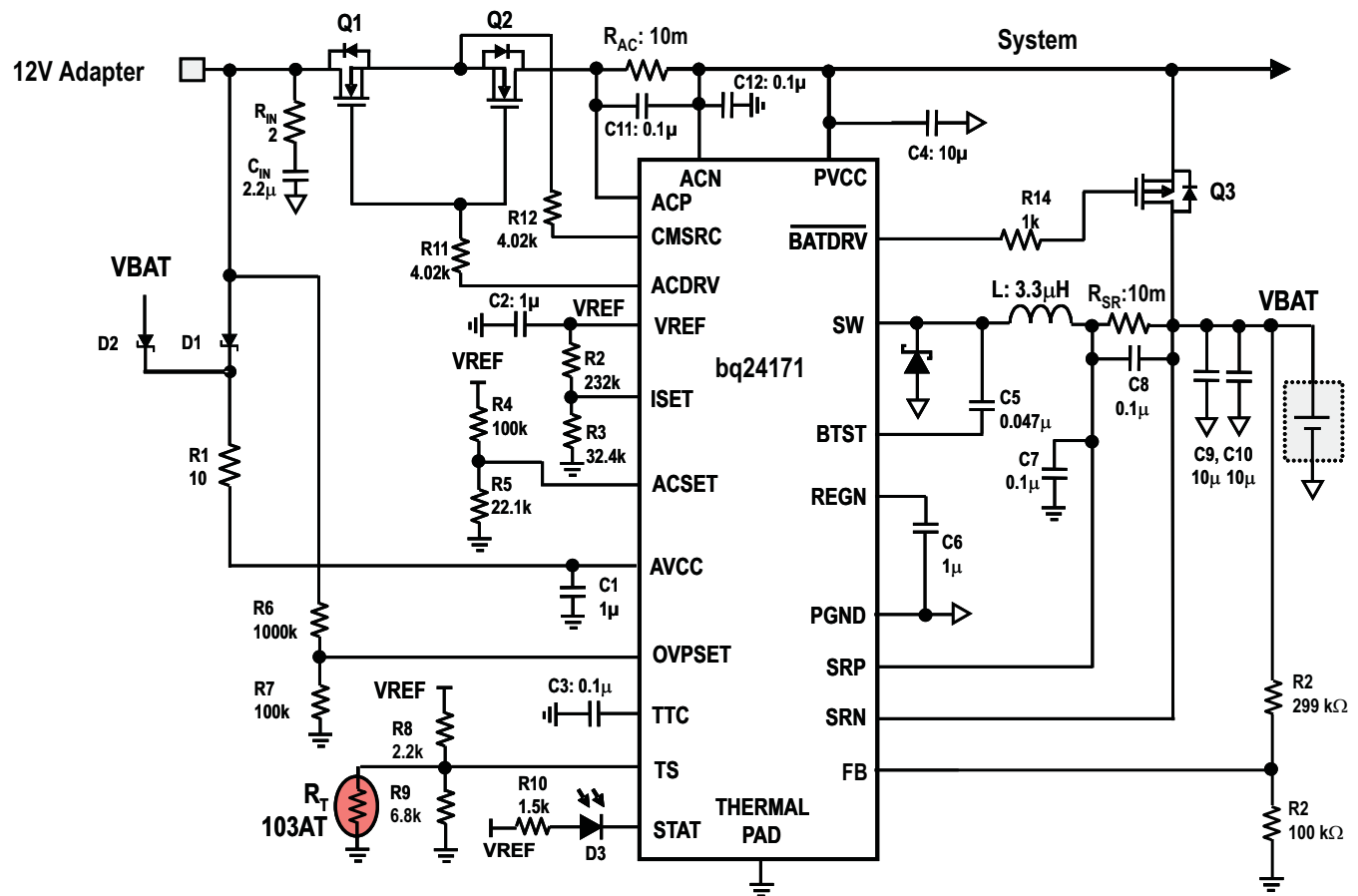


Figure 1. Typical Application Schematic (12V input, 2 cell battery 8.4V, 2A charge current, 0.2A pre-charge/termination current, 3A DPM current, 18V input OVP)



| PART NUMBER | PART MARKING | PACKAGE                | ORDERING NUMBER | QUANTITY |
|-------------|--------------|------------------------|-----------------|----------|
| bq24171     | bq24171      | 24-Pin 3.5mm×5.5mm QFN | bq24171RGYR     | 3000     |
|             |              |                        | bq24171RGYT     | 250      |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS**over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)</sup>

|   |                                    | VALUE       | UNIT |
|---|------------------------------------|-------------|------|
| Voltage range (with respect to AGND)        | AVCC, ACP, ACN, ACDRV, CMSRC, STAT | –0.3 to 30  | V    |
|   | PVCC                               | –0.3 to 20  |      |
|   | BATDRV, SRP, SRN                   | –0.3 to 20  |      |
|   | SW                                 | –2 to 20    |      |
|   | FB                                 | –0.3 to 16  |      |
|   | OVPSET, REGN, TS, TTC              | –0.3 to 7   |      |
|   | VREF, ISET, ACSET                  | –0.3 to 3.6 |      |
|   | PGND                               | –0.3 to 0.3 |      |
| Maximum difference voltage                  | SRP–SRN, ACP–ACN                   | –0.5 to 0.5 | V    |
| Junction temperature range, T <sub>J</sub>  |                                    | –40 to 155  | °C   |
| Storage temperature range, T <sub>stg</sub> |                                    | –55 to 155  | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

**THERMAL INFORMATION**

| THERMAL METRIC <sup>(1)</sup> |   | bq24171 | UNITS |
|-------------------------------|---|---------|-------|
|                               |   | RGY     |       |
|                               |   | 24 PINS |       |
| θ <sub>JA</sub>               | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 35.7    | °C/W  |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter <sup>(3)</sup>   | 0.4     |       |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter <sup>(4)</sup> | 31.2    |       |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (4) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).

**RECOMMENDED OPERATING CONDITIONS**

|  |                  | MIN  | MAX  | UNIT |
|--|------------------|------|------|------|
| Input voltage  | V <sub>IN</sub>  | 4.5  | 17   | V    |
| Output voltage                                       | V <sub>OUT</sub> |      | 13.5 | V    |
| Output current (R <sub>SR</sub> 10mΩ)                | I <sub>OUT</sub> | 0.6  | 4    | A    |
| Maximum difference voltage                           | ACP - ACN        | –200 | 200  | mV   |
|  | SRP–SRN          | –200 | 200  | mV   |
| Operation free-air temperature range, T <sub>A</sub> |                  | –40  | 85   | °C   |

**ELECTRICAL CHARACTERISTICS**

$4.5V \leq V(PVCC, AVCC) \leq 17V$ ,  $-40^{\circ}C < T_J + 125^{\circ}C$ , typical values are at  $T_A = 25^{\circ}C$ , with respect to AGND (unless otherwise noted)

| PARAMETER                        |   | TEST CONDITIONS  | MIN   | TYP                | MAX   | UNITS |
|----------------------------------|---|--|-------|--------------------|-------|-------|
| OPERATING CONDITIONS             |   |  |       |                    |       |       |
| V <sub>AVCC_OP</sub>             | AVCC input voltage operating range during charging                      |  | 4.5   |                    | 17    | V     |
| QUIESCENT CURRENTS               |   |  |       |                    |       |       |
| I <sub>BAT</sub>                 | Battery discharge current (sum of currents into AVCC, PVCC, ACP, ACN)   | V <sub>AVCC</sub> > V <sub>UVLO</sub> , V <sub>SRN</sub> > V <sub>AVCC</sub> (SLEEP), T <sub>J</sub> = 0°C to 85°C                                       |       |                    | 15    | µA    |
|                                  |   | BTST, SW, SRP, SRN, V <sub>AVCC</sub> > V <sub>UVLO</sub> , V <sub>AVCC</sub> > V <sub>SRN</sub> , ISET < 40mV, V <sub>BAT</sub> =12.6V, Charge disabled |       |                    | 25    |       |
|                                  |   | BTST, SW, SRP, SRN, V <sub>AVCC</sub> > V <sub>UVLO</sub> , V <sub>AVCC</sub> > V <sub>SRN</sub> , ISET > 120mV, V <sub>BAT</sub> =12.6V, Charge done    |       |                    | 25    |       |
| I <sub>AC</sub>                  | Adapter supply current (sum of current into AVCC,ACP, ACN)              | V <sub>AVCC</sub> > V <sub>UVLO</sub> , V <sub>AVCC</sub> > V <sub>SRN</sub> , ISET < 40mV, V <sub>BAT</sub> =12.6V, Charge disabled                     |       | 1.2                | 1.5   | mA    |
|                                  |   | V <sub>AVCC</sub> > V <sub>UVLO</sub> , V <sub>AVCC</sub> > V <sub>SRN</sub> , ISET > 120mV, Charge enabled, no switching                                |       | 2.5                | 5     |       |
|                                  |   | V <sub>AVCC</sub> > V <sub>UVLO</sub> , V <sub>AVCC</sub> > V <sub>SRN</sub> , ISET > 120mV, Charge enabled, switching                                   |       | 15 <sup>(1)</sup>  |       |       |
| CHARGE VOLTAGE REGULATION        |   |  |       |                    |       |       |
| V <sub>FB_REG</sub>              | Feedback Regulation Voltage   | V <sub>T3</sub> < V <sub>TS</sub> < V <sub>T1</sub>  |       | 2.1                |       | V     |
|                                  |   | V <sub>T4</sub> < V <sub>TS</sub> < V <sub>T3</sub>  |       | 2.05               |       |       |
|                                  |   | V <sub>T5</sub> < V <sub>TS</sub> < V <sub>T4</sub>  |       | 2.025              |       |       |
|                                  | Charge Voltage Regulation Accuracy                                      | T <sub>J</sub> = 0 to 85°C   | -0.5% |                    | -0.5% |       |
|                                  |   | T <sub>J</sub> = -40 to 125°C  | -0.7% |                    | -0.7% |       |
| I <sub>VFB</sub>                 | Leakage Current into FB pin   | V <sub>FB</sub> = 2.1V, 2.05V, 2.025V  |       |                    | 100   | nA    |
| CURRENT REGULATION – FAST CHARGE |   |  |       |                    |       |       |
| V <sub>ISET</sub>                | ISET Voltage Range  | R <sub>SENSE</sub> = 10mΩ  | 0.12  |                    | 0.8   | V     |
| K <sub>ISET</sub>                | Charge Current Set Factor (Amps of Charge Current per Volt on ISET pin) | R <sub>SENSE</sub> = 10mΩ  |       | 5                  |       | A/V   |
|                                  | Charge Current Regulation Accuracy (with Schottky diode on SW)          | V <sub>SRP-SRN</sub> = 40 mV   | -4%   |                    | 4%    |       |
|                                  |   | V <sub>SRP-SRN</sub> = 20 mV   | -7%   |                    | 7%    |       |
|                                  |   | V <sub>SRP-SRN</sub> = 5 mV  | -25%  |                    | 25%   |       |
| V <sub>ISET_CD</sub>             | Charge Disable Threshold  | ISET falling   | 40    | 50                 |       | mV    |
| V <sub>ISET_CE</sub>             | Charge Enable Threshold   | ISET rising  |       | 100                | 120   | mV    |
| I <sub>ISET</sub>                | Leakage Current into ISET   | V <sub>ISET</sub> = 2V   |       |                    | 100   | nA    |
| INPUT CURRENT REGULATION         |   |  |       |                    |       |       |
| K <sub>DPM</sub>                 | Input DPM Current Set Factor (Amps of Input Current per Volt on ACSET)  | R <sub>SENSE</sub> = 10mΩ  |       | 5                  |       | A/V   |
|                                  | Input DPM Current Regulation Accuracy (with Schottky diode on SW)       | V <sub>ACP-ACN</sub> = 80 mV   | -4%   |                    | 4%    |       |
|                                  |   | V <sub>ACP-ACN</sub> = 40 mV   | -9%   |                    | 9%    |       |
|                                  |   | V <sub>ACP-ACN</sub> = 20 mV   | -15%  |                    | 15%   |       |
|                                  |   | V <sub>ACP-ACN</sub> = 5 mV  | -20%  |                    | 20%   |       |
|                                  |   | V <sub>ACP-ACN</sub> = 2.5 mV  | -40%  |                    | 40%   |       |
| I <sub>ACSET</sub>               | Leakage Current into ACSET pin  | V <sub>ACSET</sub> = 2V  |       |                    | 100   | nA    |
| CURRENT REGULATION – PRE-CHARGE  |   |  |       |                    |       |       |
| K <sub>IPRECHG</sub>             | Precharge current set factor  | Percentage of fast charge current  |       | 10% <sup>(2)</sup> |       |       |
|                                  | Precharge current regulation accuracy                                   | V <sub>SRP-SRN</sub> = 4 mV  | -25%  |                    | 25%   |       |
|                                  |   | V <sub>SRP-SRN</sub> = 2 mV  | -40%  |                    | 40%   |       |

(1) Specified by design

(2) The minimum current is 120 mA on 10m $\Omega$  sense resistor.

**ELECTRICAL CHARACTERISTICS (continued)**

4.5V ≤ V(PVCC, AVCC) ≤ 17V, −40°C < T<sub>J</sub> + 125°C, typical values are at T<sub>A</sub> = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS   | MIN  | TYP                | MAX  | UNITS |
|--|---|---|------|--------------------|------|-------|
| <b>CHARGE TERMINATION</b>                                |   |   |      |                    |      |       |
| K <sub>TERM</sub>  | Termination current set factor  | Percentage of fast charge current   |      | 10% <sup>(3)</sup> |      |       |
|  | Termination current regulation accuracy   | V <sub>SRP-SRN</sub> = 4 mV   | −25% |                    | 25%  |       |
|  |   | V <sub>SRP-SRN</sub> = 2 mV   | −40% |                    | 40%  |       |
| t <sub>TERM_DEG</sub>                                    | Deglintch time for termination (both edges)   |   |      | 100                |      | ms    |
| t <sub>QUAL</sub>  | Termination qualification time  | V <sub>SRN</sub> > V <sub>RECH</sub> and I <sub>CHG</sub> < I <sub>TERM</sub> |      | 250                |      | ms    |
| I <sub>QUAL</sub>  | Termination qualification current   | Discharge current once termination is detected                                |      | 2                  |      | mA    |
| <b>INPUT UNDER-VOLTAGE LOCK-OUT COMPARATOR (UVLO)</b>    |   |   |      |                    |      |       |
| V <sub>UVLO</sub>  | AC under-voltage rising threshold   | Measure on AVCC   | 3.4  | 3.6                | 3.8  | V     |
| V <sub>UVLO_HYS</sub>                                    | AC under-voltage hysteresis, falling  | Measure on AVCC   |      | 300                |      | mV    |
| <b>SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)</b> |   |   |      |                    |      |       |
| V <sub>SLEEP</sub>                                       | SLEEP mode threshold  | V <sub>AVCC</sub> − V <sub>SRN</sub> falling                                  | 50   | 90                 | 150  | mV    |
| V <sub>SLEEP_HYS</sub>                                   | SLEEP mode hysteresis   | V <sub>AVCC</sub> − V <sub>SRN</sub> rising                                   |      | 200                |      | mV    |
| t <sub>SLEEP_FALL_CD</sub>                               | SLEEP deglitch to disable charge  | V <sub>AVCC</sub> − V <sub>SRN</sub> falling                                  |      | 1                  |      | ms    |
| t <sub>SLEEP_FALL_FETOFF</sub>                           | SLEEP deglitch to turn off input FETs   | V <sub>AVCC</sub> − V <sub>SRN</sub> falling                                  |      | 5                  |      | ms    |
| t <sub>SLEEP_FALL</sub>                                  | Deglitch to enter SLEEP mode, disable VREF and enter low quiescent mode                   | V <sub>AVCC</sub> − V <sub>SRN</sub> falling                                  |      | 100                |      | ms    |
| t <sub>SLEEP_PWRUP</sub>                                 | Deglitch to exit SLEEP mode, and enable VREF  | V <sub>AVCC</sub> − V <sub>SRN</sub> rising                                   |      | 30                 |      | ms    |
| <b>ACN-SRN COMPARATOR</b>                                |   |   |      |                    |      |       |
| V <sub>ACN-SRN</sub>                                     | Threshold to turn on BATFET   | V <sub>ACN-SRN</sub> falling  | 150  | 220                | 300  | mV    |
| V <sub>ACN-SRN_HYS</sub>                                 | Hysteresis to turn off BATFET   | V <sub>ACN-SRN</sub> rising   |      | 100                |      | mV    |
| t <sub>BATFETOFF_DEG</sub>                               | Deglitch to turn on BATFET  | V <sub>ACN-SRN</sub> falling  |      | 2                  |      | ms    |
| t <sub>BATFETON_DEG</sub>                                | Deglitch to turn off BATFET   | V <sub>ACN-SRN</sub> rising   |      | 50                 |      | μs    |
| <b>BAT LOWV COMPARATOR</b>                               |   |   |      |                    |      |       |
| V <sub>LOWV</sub>  | Precharge to fast charge transition   | Measure on FB   | 1.43 | 1.45               | 1.47 | V     |
| V <sub>LOWV_HYS</sub>                                    | Fast charge to precharge hysteresis   | Measure on FB   |      | 100                |      | mV    |
| t <sub>pre2fas</sub>                                     | V <sub>LOWV</sub> rising deglitch   | Delay to start fast charge current  |      | 25                 |      | ms    |
| t <sub>fast2pre</sub>                                    | V <sub>LOWV</sub> falling deglitch  | Delay to start precharge current  |      | 25                 |      | ms    |
| <b>RECHARGE COMPARATOR</b>                               |   |   |      |                    |      |       |
| V <sub>RECHG</sub>                                       | Recharge Threshold, below regulation voltage limit, V <sub>FB_REG</sub> − V <sub>FB</sub> | Measure on FB   | 35   | 50                 | 65   | mV    |
| t <sub>RECH_RISE_DEG</sub>                               | V <sub>RECHG</sub> rising deglitch  | V <sub>FB</sub> decreasing below V <sub>RECHG</sub>                           |      | 10                 |      | ms    |
| t <sub>RECH_FALL_DEG</sub>                               | V <sub>RECHG</sub> falling deglitch   | V <sub>FB</sub> increasing above V <sub>RECHG</sub>                           |      | 10                 |      | ms    |
| <b>BAT OVER-VOLTAGE COMPARATOR</b>                       |   |   |      |                    |      |       |
| V <sub>OV_RISE</sub>                                     | Over-voltage rising threshold   | As percentage of V <sub>FB_REG</sub>  |      | 104%               |      |       |
| V <sub>OV_FALL</sub>                                     | Over-voltage falling threshold  | As percentage of V <sub>FB_REG</sub>  |      | 102%               |      |       |

(3) The minimum current is 120 mA on 10mΩ sense resistor.



**ELECTRICAL CHARACTERISTICS (continued)**

4.5V ≤ V(PVCC, AVCC) ≤ 17V, −40°C < T<sub>J</sub> + 125°C, typical values are at T<sub>A</sub> = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER                                    |  | TEST CONDITIONS  | MIN   | TYP                    | MAX   | UNITS |
|--|--|--|-------|------------------------|-------|-------|
| <b>INPUT OVER-VOLTAGE COMPARATOR (ACOV)</b>  |  |  |       |                        |       |       |
| V <sub>ACOV</sub>                            | AC Over-Voltage Rising Threshold to turn off ACFET   | OVPSET rising  | 1.57  | 1.6                    | 1.63  | V     |
| V <sub>ACOV_HYS</sub>                        | AC over-voltage falling hysteresis   | OVPSET falling   |       | 50                     |       | mV    |
| t <sub>ACOV_RISE_DEG</sub>                   | AC Over-Voltage Rising Deglitch to turn off ACFET and Disable Charge   | OVPSET rising  |       | 1                      |       | μs    |
| t <sub>ACOV_FALL_DEG</sub>                   | AC Over-Voltage Falling Deglitch to Turn on ACFET  | OVPSET falling   |       | 30                     |       | ms    |
| <b>INPUT UNDER-VOLTAGE COMPARATOR (ACUV)</b> |  |  |       |                        |       |       |
| V <sub>ACUV</sub>                            | AC Under-Voltage Falling Threshold to turn off ACFET   | OVPSET falling   | 0.487 | 0.497                  | 0.507 | V     |
| V <sub>ACUV_HYS</sub>                        | AC Under-Voltage Rising Hysteresis   | OVPSET rising  |       | 100                    |       | mV    |
| t <sub>ACOV_FALL_DEG</sub>                   | AC Under-Voltage Falling Deglitch to turn off ACFET and Disable Charge   | OVPSET falling   |       | 1                      |       | μs    |
| t <sub>ACOV_RISE_DEG</sub>                   | AC Under-Voltage Rising Deglitch to turn on ACFET  | OVPSET rising  |       | 30                     |       | ms    |
| <b>THERMAL REGULATION</b>                    |  |  |       |                        |       |       |
| T <sub>J_REG</sub>                           | Junction Temperature Regulation Accuracy   | ISET > 120mV, Charging   |       | 120                    |       | °C    |
| <b>THERMAL SHUTDOWN COMPARATOR</b>           |  |  |       |                        |       |       |
| T <sub>SHUT</sub>                            | Thermal shutdown rising temperature  | Temperature rising   |       | 150                    |       | °C    |
| T <sub>SHUT_HYS</sub>                        | Thermal shutdown hysteresis  | Temperature falling  |       | 20                     |       | °C    |
| t <sub>SHUT_RISE_DEG</sub>                   | Thermal shutdown rising deglitch   | Temperature rising   |       | 100                    |       | μs    |
| t <sub>SHUT_FALL_DEG</sub>                   | Thermal shutdown falling deglitch  | Temperature falling  |       | 10                     |       | ms    |
| <b>THERMISTOR COMPARATOR</b>                 |  |  |       |                        |       |       |
| V <sub>T1</sub>                              | T1 (0 °C) threshold, Charge suspended below this temperature.  | V <sub>TS</sub> rising, As Percentage to V <sub>VREF</sub>   | 70.2% | 70.8%                  | 71.4% |       |
| V <sub>T1-HYS</sub>                          | Charge back to I <sub>CHARGE</sub> /2 and V <sub>FB</sub> =2.1 V above this temperature.                       | Hysteresis, V <sub>TS</sub> falling  |       | 0.6%                   |       |       |
| V <sub>T2</sub>                              | T2 (10 °C) threshold, Charge back to I <sub>CHARGE</sub> /2 and V <sub>FB</sub> =2.1 V below this temperature. | V <sub>TS</sub> rising, As Percentage to V <sub>VREF</sub>   | 68.0% | 68.6%                  | 69.2% |       |
| V <sub>T2-HYS</sub>                          | Charge back to I <sub>CHARGE</sub> and V <sub>FB</sub> =2.1 V above this temperature.                          | Hysteresis, V <sub>TS</sub> falling  |       | 0.8%                   |       |       |
| V <sub>T3</sub>                              | T3 (45 °C) threshold, Charge back to I <sub>CHARGE</sub> and V <sub>FB</sub> =2.05 V above this temperature.   | V <sub>TS</sub> falling, As Percentage to V <sub>VREF</sub>  | 55.5% | 56.1%                  | 56.7% |       |
| V <sub>T3-HYS</sub>                          | Charge back to I <sub>CHARGE</sub> and V <sub>FB</sub> =2.1 V below this temperature.                          | Hysteresis, V <sub>TS</sub> rising   |       | 0.8%                   |       |       |
| V <sub>T4</sub>                              | T4 (50 °C) threshold, Charge back to I <sub>CHARGE</sub> and V <sub>FB</sub> =2.025 V above this temperature.  | V <sub>TS</sub> falling, As Percentage to V <sub>VREF</sub>  | 53.2% | 53.7%                  | 54.2% |       |
| V <sub>T4-HYS</sub>                          | Charge back to I <sub>CHARGE</sub> and V <sub>FB</sub> =2.05 V below this temperature.                         | Hysteresis, V <sub>TS</sub> rising   |       | 0.8%                   |       |       |
| V <sub>T5</sub>                              | T5 (60 °C) threshold, Charge suspended above this temperature.   | V <sub>TS</sub> falling, As Percentage to V <sub>VREF</sub>  | 47.6% | 48.1%                  | 48.6% |       |
| V <sub>T5-HYS</sub>                          | Charge back to I <sub>CHARGE</sub> and V <sub>FB</sub> =2.025 V below this temperature.                        | Hysteresis, V <sub>TS</sub> rising   |       | 1.2%                   |       |       |
|  | Deglitch time for Temperature Out of Valid Charge Range Detection  | V <sub>TS</sub> < V <sub>T5</sub> or V <sub>TS</sub> > V <sub>T1</sub>   |       | 400                    |       | ms    |
|  | Deglitch time for Temperature In Valid Range Detection   | V <sub>TS</sub> > V <sub>T5</sub> + V <sub>T5_HYS</sub> or V <sub>TS</sub> < V <sub>T1</sub> - V <sub>T1_HYS</sub> |       | 20                     |       |       |
|  | Deglitch time for Temperature Detection above/below T2, T3, T4 threshold                                       |  |       | 25                     |       | ms    |
|  | Charge Current when V <sub>TS</sub> between V <sub>T1</sub> and V <sub>T2</sub> range                          |  |       | I <sub>CHARGE</sub> /2 |       |       |

**ELECTRICAL CHARACTERISTICS (continued)**

4.5V ≤ V(PVCC, AVCC) ≤ 17V, −40°C < T<sub>J</sub> + 125°C, typical values are at T<sub>A</sub> = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS   | MIN   | TYP                | MAX   | UNITS  |
|---|--|---|-------|--------------------|-------|--------|
| <b>CHARGE OVER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)</b>  |  |   |       |                    |       |        |
| V <sub>OCP_CHRG</sub>                                   | Charge Over-Current Rising Threshold, V <sub>SRP</sub> > 2.2V      | Current as percentage of fast charge current  |       | 160%               |       |        |
| V <sub>OCP_MIN</sub>                                    | Charge Over-Current Limit Min, V <sub>SRP</sub> < 2.2V             | Measure V <sub>SRP-SRN</sub>  |       | 45                 |       | mV     |
| V <sub>OCP_MAX</sub>                                    | Charge Over-Current Limit Max, V <sub>SRP</sub> > 2.2V             | Measure V <sub>SRP-SRN</sub>  |       | 75                 |       | mV     |
| <b>HSFET OVER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)</b>   |  |   |       |                    |       |        |
| I <sub>OCP_HSFET</sub>                                  | Current limit on HSFET   | Measure on HSFET  | 8     | 11.5               |       | A      |
| <b>CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)</b> |  |   |       |                    |       |        |
| V <sub>UCP</sub>  | Charge under-current falling threshold                             | Measure on V <sub>(SRP-SRN)</sub>   | 1     | 5                  | 9     | mV     |
| <b>BAT SHORT COMPARATOR</b>                             |  |   |       |                    |       |        |
| V <sub>BATSH</sub>                                      | Battery short falling threshold                                    | Measure on SRN  |       | 2                  |       | V      |
| V <sub>BATSH_HYS</sub>                                  | Battery short rising hysteresis                                    | Measure on SRN  |       | 200                |       | mV     |
| t <sub>BATSH_DEG</sub>                                  | Deglitch on both edges   |   |       | 1                  |       | μs     |
| V <sub>BATSH</sub>                                      | Charge Current during BATSHORT                                     | Percentage of fast charge current   |       | 10% <sup>(4)</sup> |       |        |
| <b>VREF REGULATOR</b>                                   |  |   |       |                    |       |        |
| V <sub>VREF_REG</sub>                                   | VREF regulator voltage   | V <sub>AVCC</sub> > V <sub>UVLO</sub> , No load   | 3.267 | 3.3                | 3.333 | V      |
| I <sub>VREF_LIM</sub>                                   | VREF current limit   | V <sub>VREF</sub> = 0 V, V <sub>AVCC</sub> > V <sub>UVLO</sub>  | 35    |                    | 90    | mA     |
| <b>REGN REGULATOR</b>                                   |  |   |       |                    |       |        |
| V <sub>REGN_REG</sub>                                   | REGN regulator voltage   | V <sub>AVCC</sub> > 10 V, I <sub>SET</sub> > 120 mV   | 5.7   | 6.0                | 6.3   | V      |
| I <sub>REGN_LIM</sub>                                   | REGN current limit   | V <sub>REGN</sub> = 0 V, V <sub>AVCC</sub> > 10 v, I <sub>SET</sub> > 120 mV                                  | 40    |                    | 120   | mA     |
| <b>TTC INPUT</b>  |  |   |       |                    |       |        |
| t <sub>prechg</sub>                                     | Precharge Safety Timer   | Precharge time before fault occurs  | 1620  | 1800               | 1980  | Sec    |
| t <sub>fastchg</sub>                                    | Fast Charge Timer Range  | T <sub>chg</sub> = C <sub>TTC</sub> * K <sub>TTC</sub>  | 1     |                    | 10    | hr     |
|   | Fast Charge Timer Accuracy   |   | -10%  |                    | 10%   |        |
| K <sub>TTC</sub>  | Timer Multiplier   |   |       | 5.6                |       | min/nF |
| V <sub>TTC_LOW</sub>                                    | TTC Low Threshold  | TTC falling   |       |                    | 0.4   | V      |
| I <sub>TTC</sub>  | TTC Source/Sink Current  |   | 45    | 50                 | 55    | μA     |
| V <sub>TTC_OSC_HI</sub>                                 | TTC oscillator high threshold                                      |   |       | 1.5                |       | V      |
| V <sub>TTC_OSC_LO</sub>                                 | TTC oscillator low threshold                                       |   |       | 1                  |       | V      |
| <b>BATTERY SWITCH (BATFET) DRIVER</b>                   |  |   |       |                    |       |        |
| R <sub>DS_BAT_OFF</sub>                                 | BATFET Turn-off Resistance   | V <sub>AVCC</sub> > 5V  |       |                    | 100   | Ω      |
| R <sub>DS_BAT_ON</sub>                                  | BATFET Turn-on Resistance  | V <sub>AVCC</sub> > 5V  |       |                    | 20    | kΩ     |
| V <sub>BATDRV_REG</sub>                                 | BATFET Drive Voltage   | V <sub>BATDRV_REG</sub> = V <sub>ACN</sub> - V <sub>BATDRV</sub> when V <sub>AVCC</sub> > 5V and BATFET is on | 4.2   |                    | 7     | V      |
| t <sub>BATFET_DEG</sub>                                 | BATFET Power-up Delay to turn off BATFET after adapter is detected |   |       | 30                 |       | ms     |
| <b>AC SWITCH (ACFET) DRIVER</b>                         |  |   |       |                    |       |        |
| I <sub>ACFET</sub>                                      | ACDRV Charge Pump Current Limit                                    | V <sub>ACDRV</sub> - V <sub>CMSRC</sub> = 5V  |       | 60                 |       | μA     |
| V <sub>ACDRV_REG</sub>                                  | Gate Drive Voltage on ACFET  | V <sub>ACDRV</sub> - V <sub>CMSRC</sub> when V <sub>AVCC</sub> > V <sub>UVLO</sub>                            | 4.2   | 6                  |       | V      |
| R <sub>ACDRV_LOAD</sub>                                 | Maximum load between ACDRV and CMSRC                               |   | 500   |                    |       | kΩ     |
| <b>AC/BAT SWITCH DRIVER TIMING</b>                      |  |   |       |                    |       |        |
| t <sub>DRV_DEAD</sub>                                   | Driver Dead Time   | Dead Time when switching between ACFET and BATFET   |       | 10                 |       | μs     |

(4) The minimum current is 120 mA on 10mΩ sense resistor.

**ELECTRICAL CHARACTERISTICS (continued)**

4.5V ≤ V(PVCC, AVCC) ≤ 17V, −40°C < T<sub>J</sub> + 125°C, typical values are at T<sub>A</sub> = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER  |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNITS |
|--|--|---|------|------|------|-------|
| BATTERY DETECTION  |  |   |      |      |      |       |
| t <sub>WAKE</sub>  | Wake timer   | Max time charge is enabled  |      | 500  |      | ms    |
| I <sub>WAKE</sub>  | Wake current   | R <sub>SENSE</sub> = 10 mΩ  | 50   | 125  | 200  | mA    |
| t <sub>DISCHARGE</sub>                                   | Discharge timer  | Max time discharge current is applied   |      | 1    |      | sec   |
| I <sub>DISCHARGE</sub>                                   | Discharge current  |   |      | 8    |      | mA    |
| I <sub>FAULT</sub>                                       | Fault current after a timeout fault  |   |      | 2    |      | mA    |
| V <sub>WAKE</sub>  | Wake threshold with respect to V <sub>REG</sub> To detect battery absent during WAKE | Measure on FB   |      | 50   |      | mV    |
| V <sub>DISCH</sub>                                       | Discharge Threshold to detect battery absent during discharge                        | Measure on FB   |      | 1.45 |      | V     |
| INTERNAL PWM   |  |   |      |      |      |       |
| f <sub>sw</sub>  | PWM Switching Frequency  |   | 1360 | 1600 | 1840 | kHz   |
| t <sub>SW_DEAD</sub>                                     | Driver Dead Time <sup>(5)</sup>  | Dead time when switching between LSFET and HSFET no load  |      | 30   |      | ns    |
| R <sub>DS_HI</sub>                                       | High Side MOSFET On Resistance   | V <sub>BTST</sub> – V <sub>SW</sub> = 4.5 V   |      | 25   | 45   | mΩ    |
| R <sub>DS_LO</sub>                                       | Low Side MOSFET On Resistance  |   |      | 60   | 110  | mΩ    |
| V <sub>BTST_REFRESH</sub>                                | Bootstrap Refresh Comparator Threshold Voltage                                       | V <sub>BTST</sub> – V <sub>SW</sub> when low side refresh pulse is requested, V <sub>AVCC</sub> =4.5V | 3    |      |      | V     |
|  |  | V <sub>BTST</sub> – V <sub>SW</sub> when low side refresh pulse is requested, V <sub>AVCC</sub> >6V   | 4    |      |      |       |
| INTERNAL SOFT START (8 steps to regulation current ICHG) |  |   |      |      |      |       |
| SS_STEP  | Soft start steps   |   |      | 8    |      | step  |
| T <sub>SS_STEP</sub>                                     | Soft start step time   |   |      | 1.6  | 3    | ms    |
| CHARGER SECTION POWER-UP SEQUENCING                      |  |   |      |      |      |       |
| t <sub>CE_DELAY</sub>                                    | Delay from ISET above 120mV to start charging battery                                |   |      | 1.5  |      | s     |
| INTEGRATED BTST DIODE                                    |  |   |      |      |      |       |
| V <sub>F</sub>   | Forward Bias Voltage   | I <sub>F</sub> =120mA at 25°C   |      | 0.85 |      | V     |
| V <sub>R</sub>   | Reverse breakdown voltage  | I <sub>R</sub> =2uA at 25°C   |      |      | 20   | V     |
| LOGIC IO PIN CHARACTERISTICS                             |  |   |      |      |      |       |
| V <sub>OUT_LO</sub>                                      | STAT Output Low Saturation Voltage   | Sink Current = 5 mA   |      |      | 0.5  | V     |

(5) Specified by design

## TYPICAL CHARACTERISTICS

Table 1. Table of Graphs<sup>(1)</sup>

| FIGURE                    | DESCRIPTION                                  |
|---------------------------|--|
| <a href="#">Figure 3</a>  | AVCC, VREF, ACDRV and STAT Power Up (ISET=0) |
| <a href="#">Figure 4</a>  | Charge Enable by ISET                        |
| <a href="#">Figure 5</a>  | Current Soft Start                           |
| <a href="#">Figure 6</a>  | Charge Disable by ISET                       |
| <a href="#">Figure 7</a>  | Continuous Conduction Mode Switching         |
| <a href="#">Figure 8</a>  | Discontinuous Conduction Mode Switching      |
| <a href="#">Figure 9</a>  | BATFET to ACFET Transition during Power Up   |
| <a href="#">Figure 10</a> | System Load Transient (Input Current DPM)    |
| <a href="#">Figure 11</a> | Battery Insertion and Removal                |
| <a href="#">Figure 12</a> | Battery to Ground Short Protection           |
| <a href="#">Figure 13</a> | Battery to Ground Short Transition           |
| <a href="#">Figure 14</a> | Efficiency vs Output Current (VIN=15V)       |
| <a href="#">Figure 15</a> | Efficiency vs Output Current (VOUT=3.8V)     |

(1) All waveforms and data are measured on HPA610 and HPA706 EVMs.

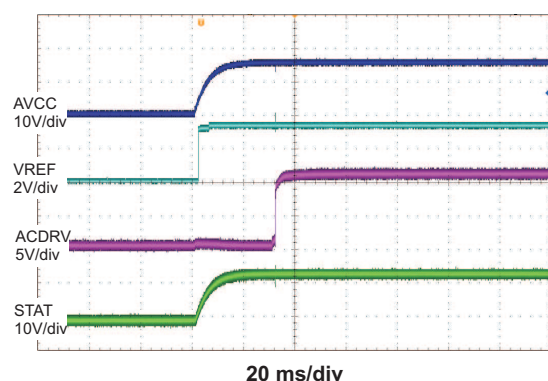


Figure 3. Power Up (ISET = 0)

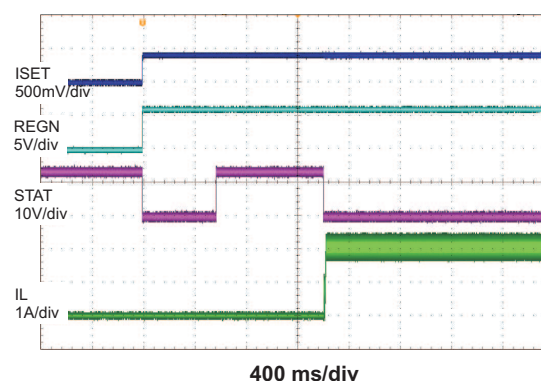


Figure 4. Charge Enable by ISET

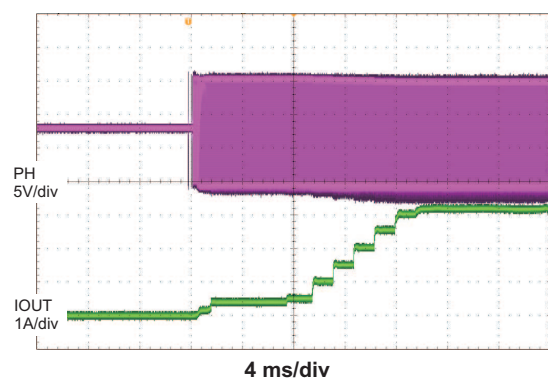


Figure 5. Current Soft Start

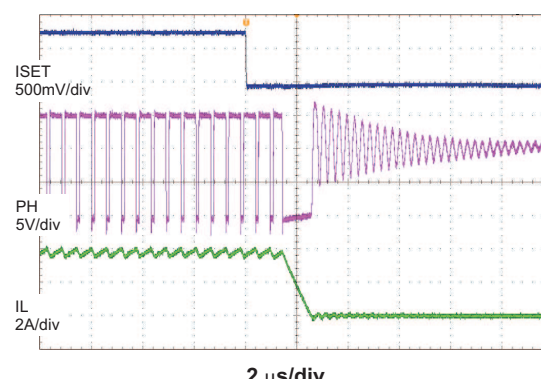
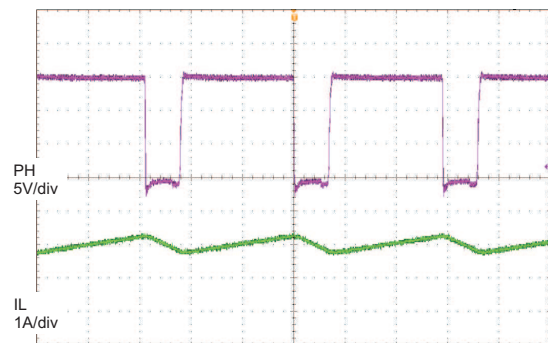
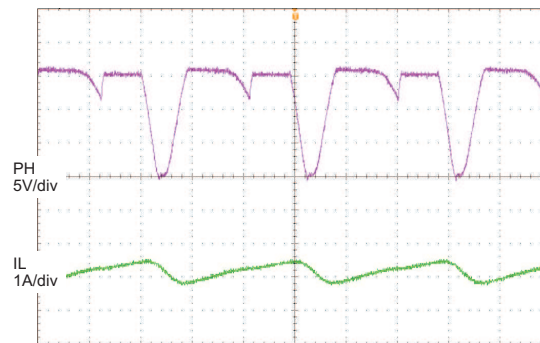


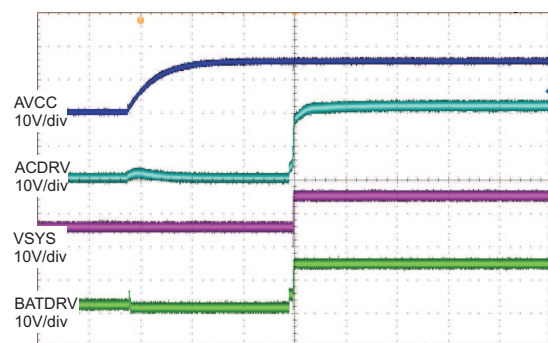
Figure 6. Charge Disable by ISET



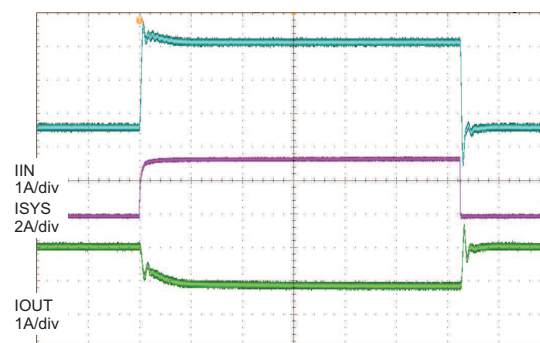
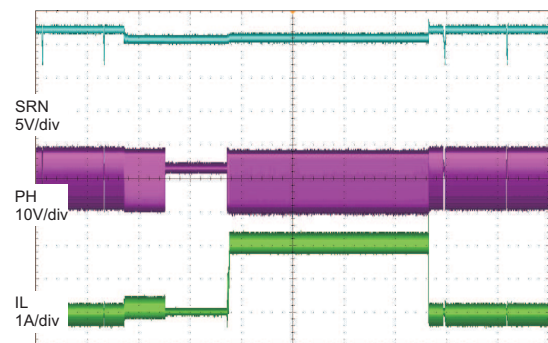
200 ns/div

**Figure 7. Continuous Conduction Mode Switching**

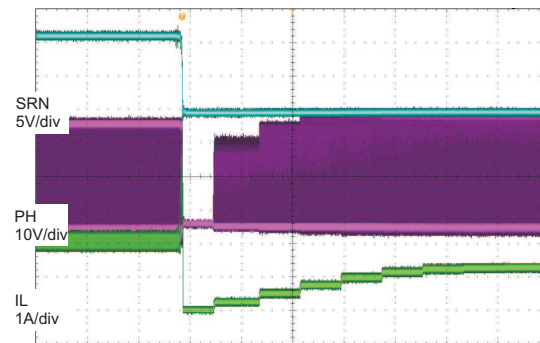
200 ns/div

**Figure 8. Discontinuous Conduction Mode Switching**

10 ms/div

**Figure 9. BATFET to ACFET Transition During Powerup**200  $\mu$ s/div**Figure 10. System Load Transient (Input current DPM)**

400 ms/div

**Figure 11. Battery Insertion and Removal**

2 ms/div

**Figure 12. Battery to Ground Short Protection**

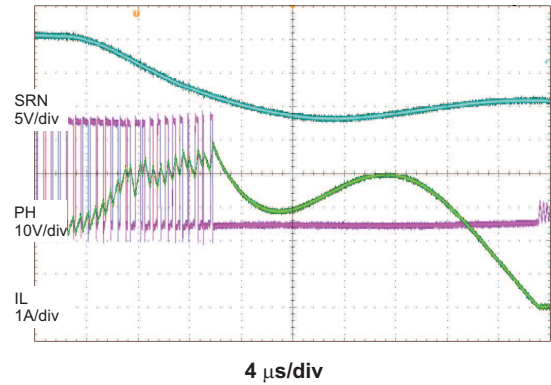


Figure 13. Battery to Ground Short Transition

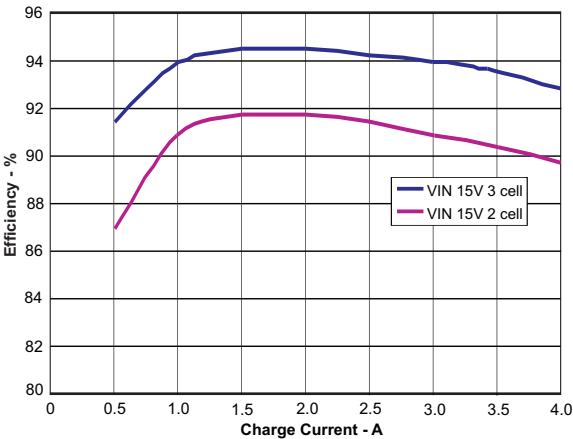


Figure 14. Efficiency vs Output Current (VIN = 15V)

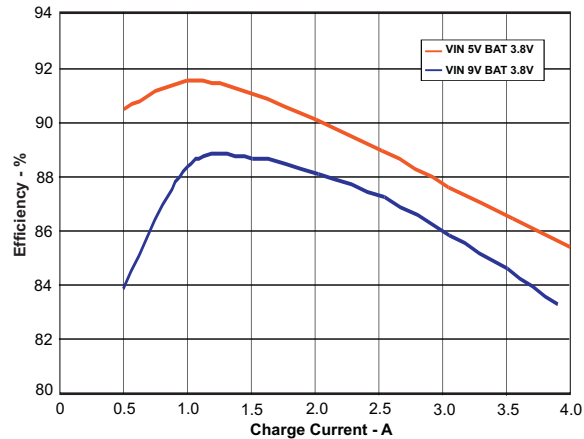


Figure 15. Efficiency vs Output Current (VOUT = 3.8V)

The schematic diagram illustrates the internal architecture of the bq24171 battery charger IC. Key components and their connections include:

- Input and Reference:** AVCC (pin 4) and VREF (pin 12) are connected to the VREF LDO. The thermal pad is connected to ground.
- System Power Selector Control:** Receives SLEEP, UVLO, ACOV, and ACUV signals. It controls the ACN-SRN and ACN-6V lines.
- ACSRV Charge Pump:** Converts CMSRC+6V to ACN and ACN-6V.
- Regulator and LDOs:** The REGN LDO (pins 20, 21) regulates the output. The VREF LDO provides a reference voltage.
- Control and Protection:** Includes a PWM CONTROL block, a LEVEL SHIFTER, and a STATE MACHINE. The STATE MACHINE manages the EN\_CHARGE signal and handles Discharge, Termination Qualification, and Suspend states.
- Timing and Thresholds:** Various comparators and op-amps set thresholds for UVLO (3.6V), SLEEP (VSRN+90mV), BAT\_OVP (2.184V), and others. The Fast Charge Timer (TTC) and Precharge Timer (30 mins) are also shown.
- Output and Monitoring:** The output is connected to the battery (BATDRV, pin 19). Monitoring points include ACN (pin 7), CMSRC (pin 8), and PGND (pins 22, 23).

### Figure 16. Functional Block Diagram

## DETAILED DESCRIPTION

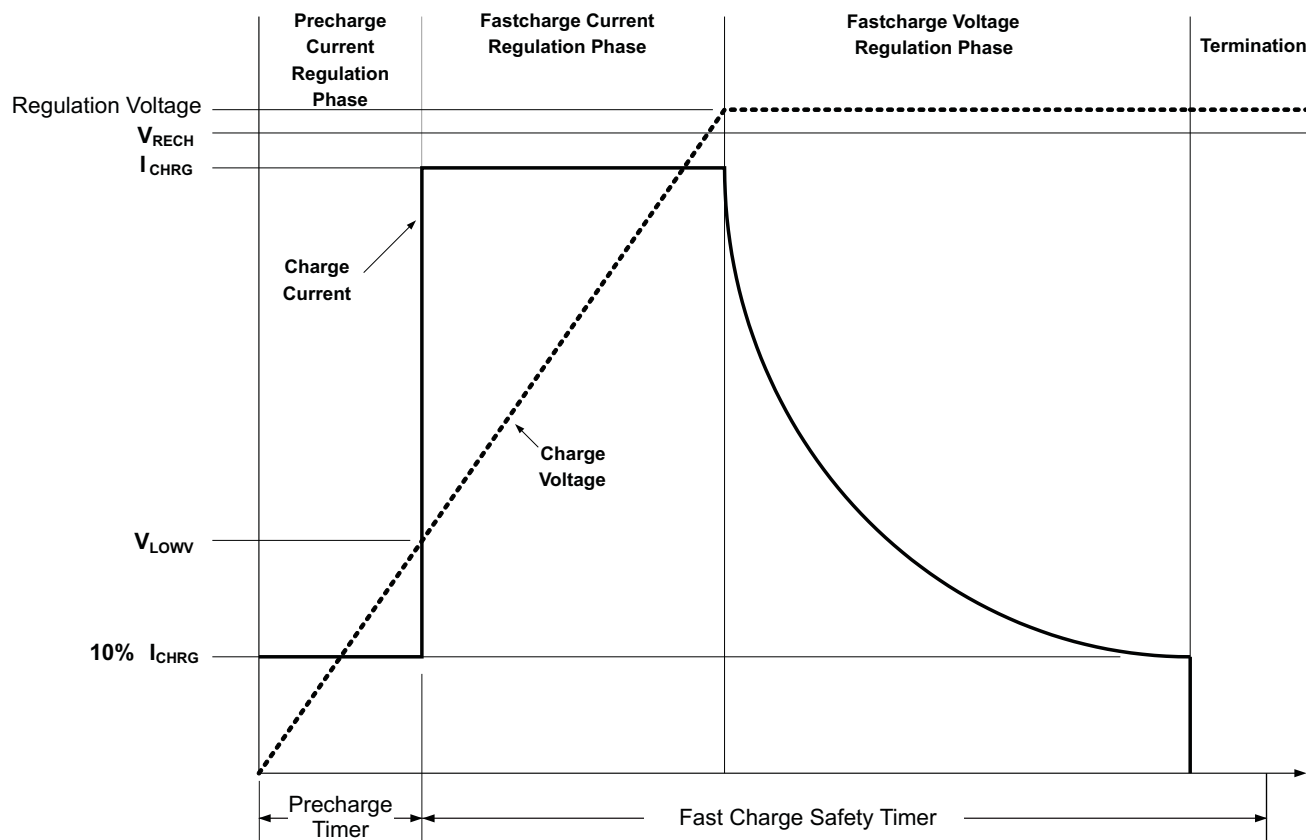


Figure 17. Typical Charging Profile

## BATTERY VOLTAGE REGULATION

The bq24171 offers a high accuracy voltage regulator on for the charging voltage.

The bq24171 uses external resistor divider for voltage feedback and regulate to internal 2.1V voltage reference on FB pin. Use the following equation for the regulation voltage for bq24171:

$$V_{BAT} = 2.1 \text{ V} \times \left[ 1 + \frac{R2}{R1} \right] \quad (1)$$

where R2 is connected from FB to the battery and R1 is connected from FB to GND.

## BATTERY CURRENT REGULATION

The ISET input sets the maximum charging current. Battery current is sensed by current sensing resistor RSR connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 40mV max. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET}}{20 \times R_{SR}} \quad (2)$$

The valid input voltage range of ISET is up to 0.8V. With 10mΩ sense resistor, the maximum output current is 4A. With 20mΩ sense resistor, the maximum output current is 2A.

The charger is disabled when ISET pin voltage is below 40mV and is enabled when ISET pin voltage is above 120mV. For 10mΩ current sensing resistor, the minimum fast charge current must be higher than 600mA.

Under high ambient temperature, the charge current will fold back to keep IC temperature not exceeding 120°C.



## BATTERY PRECHARGE CURRENT REGULATION

On Power-up, if the battery voltage is below the  $V_{LOWV}$  threshold, the bq24171 applies the pre-charge current to the battery. This pre-charge feature is intended to revive deeply discharged cells. If the  $V_{LOWV}$  threshold is not reached within 30 minutes of initiating pre-charge, the charger turns off and a FAULT is indicated on the status pins.

For bq24171, the pre-charge current is set as 10% of the fast charge rate set by ISET voltage.

$$I_{PRECHARGE} = \frac{V_{ISET}}{200 \times R_{SR}} \quad (3)$$

## INPUT CURRENT REGULATION

The total input current from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum available charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the summation of system power and charge power exceeds the maximum input power. Therefore, the current capability of the AC adapter can be lowered, reducing system cost.

Input current is set by the voltage on ACSET pin using the following equation:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \quad (4)$$

The ACP and ACN pins are used to sense across RAC with default value of 10mΩ. However, resistors of other values can also be used. A larger sense resistor will give a larger sense voltage and higher regulation accuracy, at the expense of higher conduction loss.

## CHARGE TERMINATION, RECHARGE, AND SAFETY TIMERS

The charger monitors the charging current during the voltage regulation phase. Termination is detected when the FB voltage is higher than recharge threshold and the charge current is less than the termination current threshold, as calculated below:

$$I_{TERM} = \frac{V_{ISET}}{200 \times R_{SR}} \quad (5)$$

where  $V_{ISET}$  is the voltage on the ISET pin and  $R_{SR}$  is the sense resistor. There is a 25ms deglitch time during transition between fast-charge and pre-charge.

As a safety backup, the charger also provides an internal fixed 30 minutes pre-charge safety timer and a programmable fast charge timer. The fast charge time is programmed by the capacitor connected between the TTC pin and AGND, and is given by the formula:

$$t_{TTC} = C_{TTC} \times K_{TTC} \quad (6)$$

Where  $C_{TTC}$  is the capacitor connected to TTC and  $K_{TTC}$  is the constant multiplier.

A new charge cycle is initiated when one of the following conditions occurs:

- The battery voltage falls below the recharge threshold
- A power-on-reset (POR) event occurs
- ISET pin toggled below 40mV (disable charge) and above 120mV (enable charge)

Pull TTC pin to AGND to disable both termination and fast charge safety timer (reset timer). Pull TTC pin to VREF to disable the safety timer, but allow charge termination.

## POWER UP

The charge uses a SLEEP comparator to determine the source of power on the AVCC pin, since AVCC can be supplied either from the battery or the adapter. With the adapter source present, if the AVCC voltage is greater than the SRN voltage, the charger exits SLEEP mode. If all conditions are met for charging, the charger then starts charge the battery (see **the *Enabling and Disabling Charging*** section). If SRN voltage is greater than AVCC, the charger enters low quiescent current SLEEP mode to minimize current drain from the battery. During SLEEP mode, the VREF output turns off and the STAT pin goes to high impedance.

If AVCC is below the UVLO threshold, the device is disabled.

## INPUT UNDER-VOLTAGE LOCK-OUT (UVLO)

The system must have a minimum AVCC voltage to allow proper operation. This AVCC voltage could come from either input adapter or battery, since a conduction path exists from the battery to AVCC through the high side NMOS body diode. When AVCC is below the UVLO threshold, all circuits on the IC are disabled.

## INPUT OVER-VOLTAGE/UNDER-VOLTAGE PROTECTION

ACOV provides protection to prevent system damage due to high input voltage. In bq24171, once the voltage on OVPSET is above the 1.6V ACOV threshold or below the 0.5V ACUV threshold, charge is disabled and input MOSFETs turn off. The bq24171 provides flexibility to set the input qualification threshold.

## ENABLE AND DISABLE CHARGING

The following conditions have to be valid before charging is enabled:

- ISET pin above 120mV
- Device is not in Under-Voltage-Lock-Out (UVLO) mode (i.e.  $V_{AVCC} > V_{UVLO}$ )
- Device is not in SLEEP mode (i.e.  $V_{AVCC} > V_{SRN}$ )
- OVPSET voltage is between 0.5V and 1.6V to qualify the adapter
- 1.5s delay is complete after initial power-up
- REGN LDO and VREF LDO voltages are at correct levels
- Thermal Shut down (TSHUT) is not valid
- TS fault is not detected
- ACFET turns on (See **System Power Selector** for details)

One of the following conditions stops on-going charging:

- ISET pin voltage is below 40mV
- Device is in UVLO mode
- Adapter is removed, causing the device to enter SLEEP mode
- OVPSET voltage indicates the adapter is not valid
- REGN or VREF LDO voltage is overloaded
- TSHUT temperature threshold is reached
- TS voltage goes out of range indicating the battery temperature is too hot or too cold
- ACFET turns off
- TTC timer expires or pre-charge timer expires

## SYSTEM POWER SELECTOR

The IC automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or during SLEEP mode. When the adapter plugs in and the voltage is above the battery voltage, the IC exits SLEEP mode. The battery is disconnected from the system and the adapter is connected to the system after exiting SLEEP. An automatic break-before-make logic prevents shoot-through currents when the selectors switch.

The ACDRV is used to drive a pair of back-to-back n-channel power MOSFETs between adapter and ACP with sources connected together to CMSRC. The n-channel FET with the drain connected to the ACP (Q2, RBFET) provides reverse battery discharge protection, and minimizes system power dissipation with its low-RDS<sub>ON</sub>. The other n-channel FET with drain connected to adapter input (Q1, ACFET) separates battery from adapter, and provides a limited dI/dt when connecting the adapter to the system by controlling the FET turn-on time. The /BATDRV controls a p-channel power MOSFET (Q3, BATFET) placed between battery and system with drain connected to battery.

Before the adapter is detected, the ACDRV is pulled to CMSRC to keep ACFET off, disconnecting the adapter from system. /BATDRV stays at ACN-6V (clamp to ground) to connect battery to system if all the following conditions are valid:

- $V_{AVCC} > V_{UVLO}$  (battery supplies AVCC)
- $V_{ACN} < V_{SRN} + 200 \text{ mV}$

After the device comes out of SLEEP mode, the system begins to switch from battery to adapter. The AVCC voltage has to be 300mV above SRN to enable the transition. The break-before-make logic keeps both ACFET and BATFET off for 10us before ACFET turns on. This prevents shoot-through current or any large discharging current from going into the battery. The /BATDRV is pulled up to ACN and the ACDRV pin is set to CMSRC + 6V by an internal charge pump to turn on n-channel ACFET, connecting the adapter to the system if all the following conditions are valid:

- $V_{ACUV} < V_{OVSET} < V_{ACOV}$
- $V_{AVCC} > V_{SRN} + 300 \text{ mV}$

When the adapter is removed, the IC turns off ACFET and enters SLEEP mode.

BATFET keeps off until the system drops close to SRN. The  $\overline{\text{BATDRV}}$  pin is driven to ACN - 6V by an internal regulator to turn on p-channel BATFET, connecting the battery to the system.

Asymmetrical gate drive provides fast turn-off and slow turn-on of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turn-on of both MOSFETs. The delay time can be further increased, by putting a capacitor from gate to source of the power MOSFETs.

## CONVERTER OPERATION

The bq24171 employs a 1.6MHz constant-frequency step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty-cycle of the converter. The ramp height is proportional to the AVCC voltage to cancel out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. Internal gate drive logic allows achieving 97% duty-cycle before pulse skipping starts.

## AUTOMATIC INTERNAL SOFT-START CHARGER CURRENT

The charger automatically soft-starts the charger regulation current every time the charger goes into fast-charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1.6ms, for a typical rise time of 12.8ms. No external components are needed for this function.

## CHARGE OVER-CURRENT PROTECTION

The charger monitors top side MOSFET current by high side sense FET. When peak current exceeds MOSFET limit, it will turn off the top side MOSFET and keep it off until the next cycle. The charger has a secondary cycle-to-cycle over-current protection. It monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when either over-current condition is detected, and automatically resumes when the current falls below the over-current threshold.

## CHARGE UNDER-CURRENT PROTECTION

After the recharge, if the SRP-SRN voltage decreases below 5mV, the low side FET will be turned off for the rest of the switching cycle. During discontinuous conduction mode (DCM), the low side FET will only turn on for a short period of time when the bootstrap capacitor voltage drops below 4V to provide refresh charge for the capacitor. This is important to prevent negative inductor current from causing any boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This can lead to an over-voltage on the AVCC node and potentially cause damage to the system.

## BATTERY DETECTION

For applications with removable battery packs, IC provides a battery absent detection scheme to reliably detect insertion or removal of battery packs. The battery detection routine runs on power up, or if battery voltage falls below recharge threshold voltage due to removing a battery or discharging a battery.

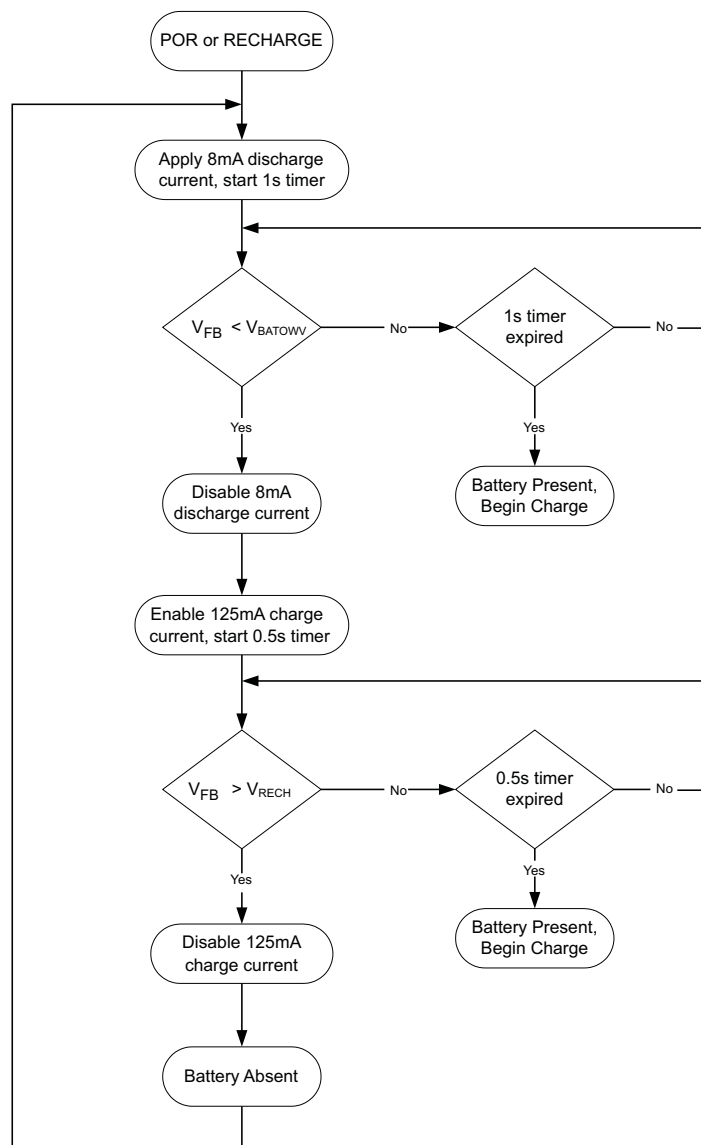


Figure 18. Battery Detection Flowchart

Once the device has powered up, a 8-mA discharge current is applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125mA). If the battery voltage gets up above the recharge threshold within 500ms, there is no battery present and the cycle restarts. If either the 500ms or 1 second timer time out before the respective thresholds are hit, a battery is detected and a charge cycle is initiated.

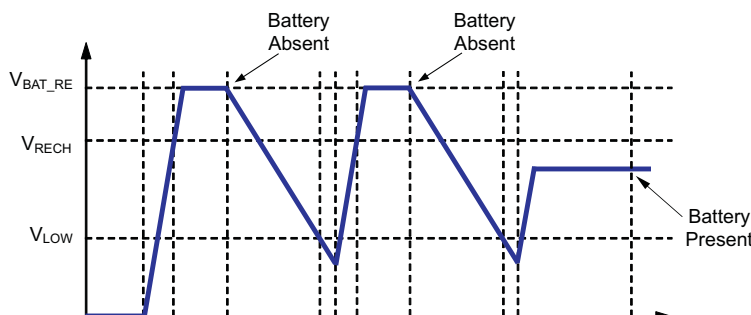


Figure 19. Battery Detect Timing Diagram

Care must be taken that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the voltage below the LOWV threshold during the 1 second discharge time. The maximum output capacitances can be calculated according to the following equation:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{(2.05 \text{ V} - 1.45 \text{ V}) \times \left[ 1 + \frac{R_2}{R_1} \right]} \quad (7)$$

Where  $C_{MAX}$  is the maximum output capacitance,  $I_{DISCH}$  is the discharge current,  $t_{DISCH}$  is the discharge time, and  $R_2$  and  $R_1$  are the voltage feedback resistors from the battery to the FB pin.

### Example

For a 3-cell Li+ charger, with  $R_2 = 500\text{k}\Omega$ ,  $R_1 = 100\text{k}\Omega$  (giving 12.6V for voltage regulation),  $I_{DISCH} = 8\text{mA}$ ,  $t_{DISCH} = 1$  second.

$$C_{MAX} = \frac{8 \text{ mA} \times 1 \text{ sec}}{0.6 \text{ V} \times \left[ 1 + \frac{500 \text{ k}\Omega}{100 \text{ k}\Omega} \right]} = 2.2 \text{ mF} \quad (8)$$

Based on these calculations, no more than 2200  $\mu\text{F}$  should be allowed on the battery node for proper operation of the battery detection circuit.

### BATTERY SHORT PROTECTION

When SRN pin voltage is lower than 2V it is considered as battery short condition during charging period. The charger will shut down immediately for 1ms, then soft start back to the charging current the same as precharge current. This prevents high current may build in output inductor and cause inductor saturation when battery terminal is shorted during charging. The converter works in non-synchronous mode during battery short.

### BATTERY OVER-VOLTAGE PROTECTION

The converter will not allow the high-side FET to turn-on until the battery voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A total 6mA current sink from SRP/SRN to AGND allows discharging the stored output inductor energy that is transferred to the output capacitors. If battery over-voltage condition lasts for more than 30ms, charge is disabled.

## TEMPERATURE QUALIFICATION AND JEITA GUIDELINE

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS pin must be within the  $V_{T1}$  to  $V_{T5}$  thresholds. If  $V_{TS}$  is outside of this range, the controller suspends charge and waits until the battery temperature is within the  $V_{T1}$  to  $V_{T5}$  range. During the charge cycle the battery temperature must be within the  $V_{T1}$  to  $V_{T5}$  thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the  $V_{T1}$  to  $V_{T5}$  range. The controller suspends charge by turning off the PWM charge FETs. If  $V_{TS}$  is within the range of  $V_{T1}$  and  $V_{T2}$ , charge voltage regulation on FB pin is 2.1 V and the charge current is reduced to  $I_{CHARGE}/2$  (To avoid early termination during  $V_{T1}$  and  $V_{T2}$  range, fast charge current need to be bigger than 2 times of termination current); if  $V_{TS}$  is within the range of  $V_{T2}$  and  $V_{T3}$ , the charge voltage regulation on FB pin is 2.1 V; if  $V_{TS}$  is within  $V_{T3}$  and  $V_{T4}$ , the charge voltage regulation on FB pin is reduced back to 2.05 V; and if  $V_{TS}$  is within  $V_{T4}$  and  $V_{T5}$ , the charge voltage regulation on FB pin is further reduced to 2.025 V. Figure 20 below summarizes the operation. See the Li-ion battery-charger solutions for JEITA compliance, [SLYT365](#)

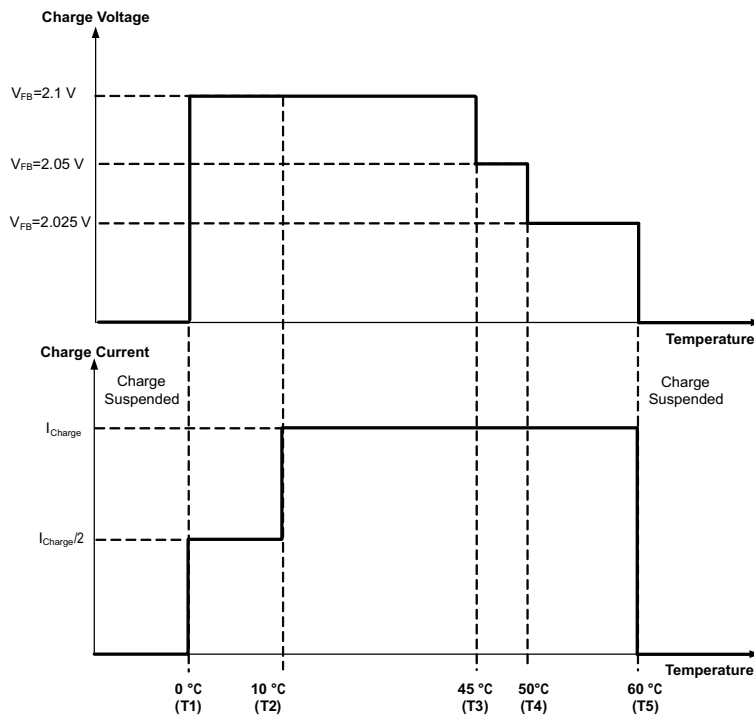
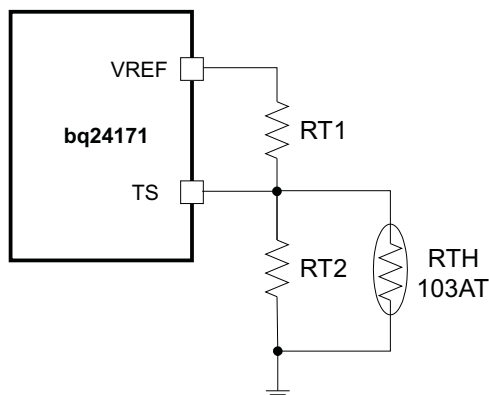


Figure 20. TS Pin, Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in [Figure 21](#), the values of  $RT1$  and  $RT2$  can be determined by using [Equation 9](#) and [Equation 10](#):

$$RT2 = \frac{V_{VREF} \times R_{TH\_COLD} \times R_{TH\_HOT} \times \left( \frac{1}{VT1} - \frac{1}{VT5} \right)}{R_{TH\_HOT} \times \left( \frac{V_{VREF}}{VT5} - 1 \right) - R_{TH\_COLD} \times \left( \frac{V_{VREF}}{VT1} - 1 \right)} \quad (9)$$

$$RT1 = \frac{\frac{V_{VREF}}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{R_{TH\_COLD}}} \quad (10)$$



**Figure 21. TS Resistor Network**

For example, 103AT NTC thermistors are used to monitor the battery pack temperature. Select  $T_1 = 0^\circ\text{C}$  for COLD and  $T_5 = 60^\circ\text{C}$  for HOT, then we get  $R_{T_2} = 6.8\text{k}\Omega$  and  $R_{T_1} = 2.2\text{k}\Omega$  as in the [design tool](#). A small RC filter is suggested to use for system-level ESD protection.

## MOSFET SHORT CIRCUIT AND INDUCTOR SHORT CIRCUIT PROTECTION

The IC has a short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across  $R_{ds(on)}$  of the MOSFETs. The charger will be latched off, but the ACFET keep on to power the system. The only way to reset the charger from latch-off status is remove adapter then plug adapter in again. Meanwhile, STAT is blinking to report the fault condition.

## THERMAL REGULATION AND SHUTDOWN PROTECTION

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. The internal thermal regulation loop will fold back the charge current to keep the junction temperature from exceeding  $120^\circ\text{C}$ . As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of  $150^\circ\text{C}$ . The charger stays off until the junction temperature falls below  $130^\circ\text{C}$ .

## TIMER FAULT RECOVERY

The IC provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: The battery voltage is above the recharge threshold and a timeout fault occurs.

Recovery Method: The timer fault will clear when the battery voltage falls below the recharge threshold, and battery detection will begin. A POR or taking ISET below 40mV will also clear the fault.

Condition 2: The battery voltage is below the recharge threshold and a timeout fault occurs.

Recovery Method: Under this scenario, the IC applies the fault current to the battery. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disabled the fault current and executes the recovery method described in Condition 1. A POR or taking ISET below 40mV will also clear the fault.

## INDUCTOR, CAPACITOR, AND SENSE RESISTOR SELECTION GUIDELINES

The IC provides internal loop compensation. With this scheme, the best stability occurs when the LC resonant frequency,  $f_o$ , is approximately 15kHz – 25kHz for the IC.

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

(11)

Table 2 provides a summary of typical LC components for various charge currents.

**Table 2. Typical Values as a Function of Charge Current**

| CHARGE CURRENT     | 1A          | 2A          | 3A          | 4A          |
|--------------------|-------------|-------------|-------------|-------------|
| Output inductor L  | 6.8 $\mu$ H | 3.3 $\mu$ H | 3.3 $\mu$ H | 2.2 $\mu$ H |
| Output capacitor C | 10 $\mu$ F  | 20 $\mu$ F  | 20 $\mu$ F  | 30 $\mu$ F  |

## CHARGE STATUS OUTPUTS

The open-drain STAT outputs indicate various charger operations as listed in Table 3. These status pins can be used to drive LEDs or communicate with the host processor. Note that OFF indicates that the open-drain transistor is turned off.

**Table 3. STAT Pin Definition**

| CHARGE STATE  | STAT  |
|---|-------|
| Charge in progress (including recharging)   | ON    |
| Charge complete, Sleep mode, Charge disabled  | OFF   |
| Charge suspend, Input over-voltage, Battery over-voltage, timer fault, , battery absent | BLINK |



## APPLICATION INFORMATION

### INDUCTOR SELECTION

The bq24171 has a 1600-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current ( $I_{CHG}$ ) plus half the ripple current ( $I_{RIPPLE}$ ):

$$I_{SAT} \geq I_{CHG} + (1/2)I_{RIPPLE} \quad (12)$$

Inductor ripple current depends on input voltage ( $V_{IN}$ ), duty cycle ( $D = V_{OUT}/V_{IN}$ ), switching frequency ( $f_s$ ), and inductance ( $L$ ):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_s \times L} \quad (13)$$

The maximum inductor ripple current happens with  $D = 0.5$  or close to 0.5. Usually inductor ripple is designed in the range of 20% to 40% of the maximum charging current as a trade-off between inductor size and efficiency for a practical design.

### INPUT CAPACITOR

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current  $I_{CIN}$  occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (14)$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25V rating or higher capacitor is preferred for a 15V input voltage. A 20 $\mu$ F capacitance is suggested for a typical 3A to 4A charging current.

### OUTPUT CAPACITOR

The output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current  $I_{COUT}$  is given as:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (15)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCf_s^2} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (16)$$

At certain input/output voltages and switching frequencies, the voltage ripple can be reduced by increasing the output filter LC.

The bq24171 has an internal loop compensator. To achieve good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 25 kHz. The preferred ceramic capacitor has a 25V or higher rating, X7R or X5R.

### INPUT FILTER DESIGN

During adapter hot plug-in, the parasitic inductance and the input capacitor from the adapter cable form a second order system. The voltage spike at the AVCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an over-voltage event on the AVCC pin.

There are several methods to damping or limiting the over-voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over-voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over-voltage level to an IC safe level. However, these two solutions may not be lowest cost or smallest size.

A cost effective and small size solution is shown in Figure 22. R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the over-voltage spike is limited to a safe level. D1 is used for reverse voltage protection for the AVCC pin. C2 is the AVCC pin decoupling capacitor and it should be placed as close as possible to the AVCC pin. R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high voltage spikes. The C2 value should be less than the C1 value so R1 can dominant the equivalent ESR value to provide enough damping effect for hot plug-in. R1 and R2 must be sized to handle in-rush current power loss according to the resistor manufacturer's datasheet. Verify the filter component values with a real application and make any minor adjustments needed to fit in the real application circuit.

If the input is 5V (USB host or USB adapter), diode D1 can be omitted. R2 must be 5Ω or higher to limit the current if the input is reversely inserted.

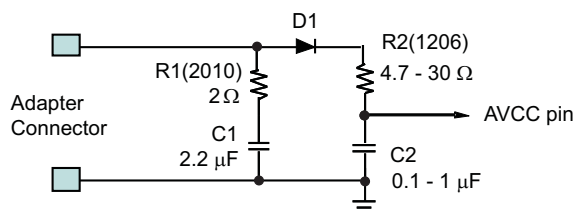


Figure 22. Input Filter

## INPUT ACFET AND RBFET SELECTION

N-type MOSFETs are used as input ACFET(Q1) and RBFET(Q2) for better cost effective and small size solution, as shown in Figure 23. Normally, there are around 50uF capacitor totally connected at PVCC node --- 10μF capacitor for buck converter of bq24171 and 40μF capacitor for system side. There is a surge current during Q1 turn-on period when a valid adapter is inserted. Decreasing the turn-on speed of Q1 can limit this surge current in desirable range by selecting a MOSFET with relative bigger  $C_{GD}$  and/or  $C_{GS}$ . At the case Q1 turn on too fast, we need add external  $C_{GD}$  and/or  $C_{GS}$ . For example, 4.7nF  $C_{GD}$  and 47nF  $C_{GS}$  are adopted on EVM while using NexFET CSD17313 as Q1.

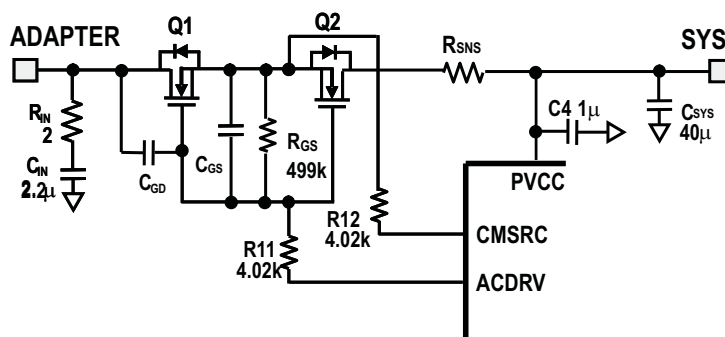


Figure 23. Input ACFET and RBFET

## PCB LAYOUT

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loop (see Figure 24) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. The following is a PCB layout priority list for proper layout. Layout of the PCB according to this specific order is essential.

1. Place input capacitor as close as possible to the PVCC supply and ground connections and use the shortest copper trace connection. These parts should be placed on the same layer of the PCB instead of on different layers and using vias to make this connection.
2. Place the inductor input terminal as close as possible to the SW terminal. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

3. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in the same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see [Figure 25](#) for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.
4. Place output capacitor next to the sensing resistor output and ground.
5. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
6. Route analog ground separately from power ground and use a single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling. Use the thermal pad as a single ground connection point to connect analog ground and power ground together, or use a 0-Ω resistor to tie analog ground to power ground. A star-connection under the thermal pad is highly recommended.
7. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
9. The number and physical size of the vias should be enough for a given current path.

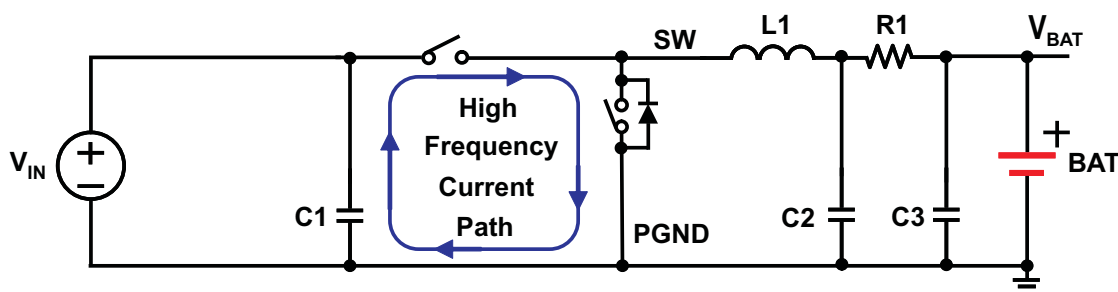


Figure 24. High Frequency Current Path

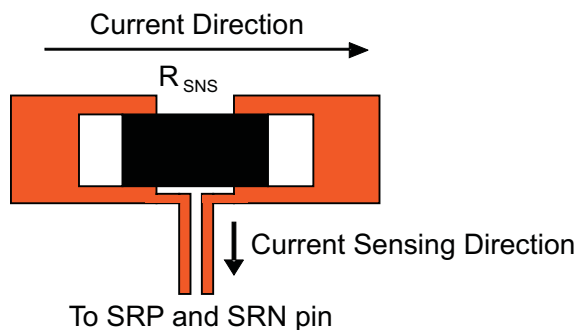


Figure 25. Sensing Resistor PCB Layout

**REVISION HISTORY**

Note: Page numbers of current version may differ from previous versions.

| <b>Changes from Original (February 2011) to Revision A</b>   | <b>Page</b> |
|--|-------------|
| • Changed publication to Rev A, May 2011 .....   | 1           |
| • Changed the 4th FEATURES bullet from "4.5V to 17V Input Operating Voltage" to "30V Input Rating with Adjustable Over-Voltage Protection" and sub-bullet "4.5V to 17V Input Operating Voltage" .....                            | 1           |
| • Added esds note to top of second page; added "DESCRIPTION (Continued)" title on second page; and new paragraph on page 2 (beginning "The bq24171 charges battery from DC source as high as 17V.") .....                        | 2           |
| • Added connection between CMSRC and ACP in Figure 2 Typical Application schematic. ....   | 5           |
| • Changed ABS MAX table first-row descriptors from "PVCC, AVCC, ACN, CMSRC, STAT" to "AVCC, ACP, ACN, ACDRV, CMSRC, STAT" and second-row descriptor from "ACDRV, BTST" to "PVCC"; changed PVCC max voltage from 30V to 20V ..... | 6           |
| • Changed hyperlink to point to Design Tool sluc244a .....   | 23          |
| • Added new paragraph under INPUT FILTER DESIGN section (beginning..."If the input is 5V....") .....   | 26          |

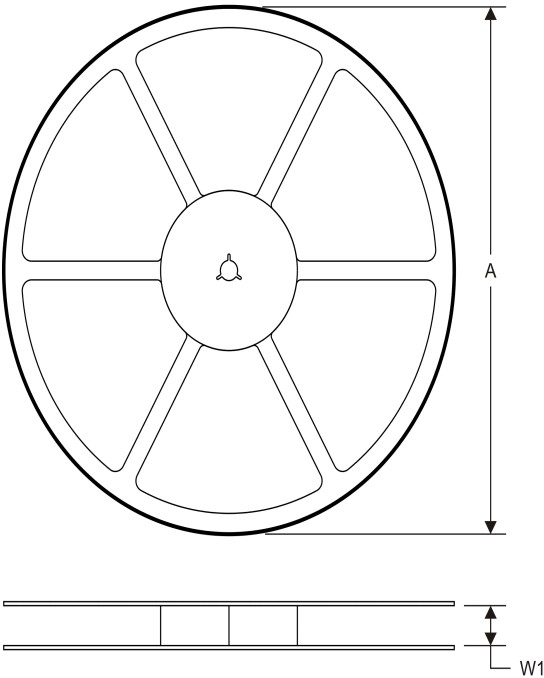
---

PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| BQ24171RGYR      | ACTIVE                | VQFN         | RGY             | 24   | 3000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-2-260C-1 YEAR          |                             |
| BQ24171RGYT      | ACTIVE                | VQFN         | RGY             | 24   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-2-260C-1 YEAR          |                             |

TAPE AND REEL INFORMATION

REEL DIMENSIONS

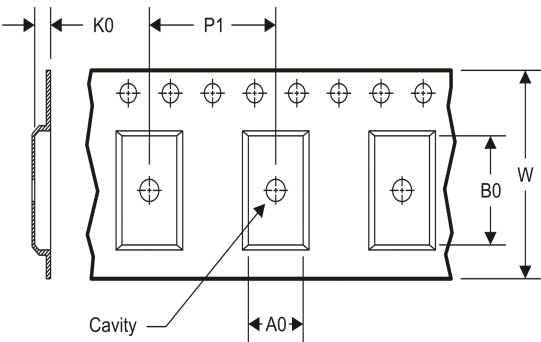


TAPE AND REEL INFORMATION

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ24171RGYR | VQFN         | RGY             | 24   | 3000 | 330.0              | 12.4               | 3.8     | 5.8     | 1.2     | 8.0     | 12.0   | Q1            |
| BQ24171RGYT | VQFN         | RGY             | 24   | 250  | 180.0              | 12.4               | 3.8     | 5.8     | 1.2     | 8.0     | 12.0   | Q1            |

TAPE DIMENSIONS

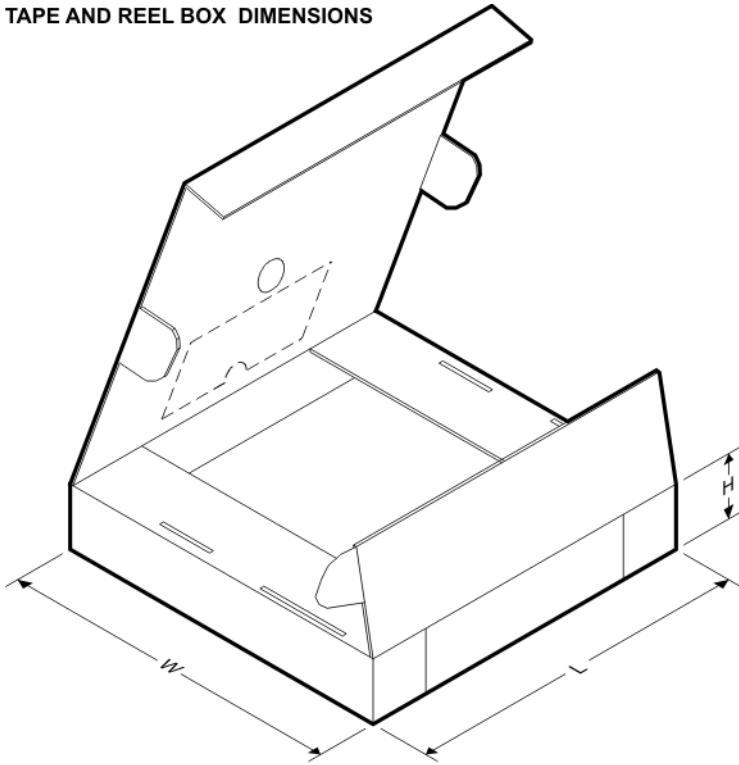


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

# PACKAGE MATERIALS INFORMATION

14-Jul-2012

## TAPE AND REEL BOX DIMENSIONS

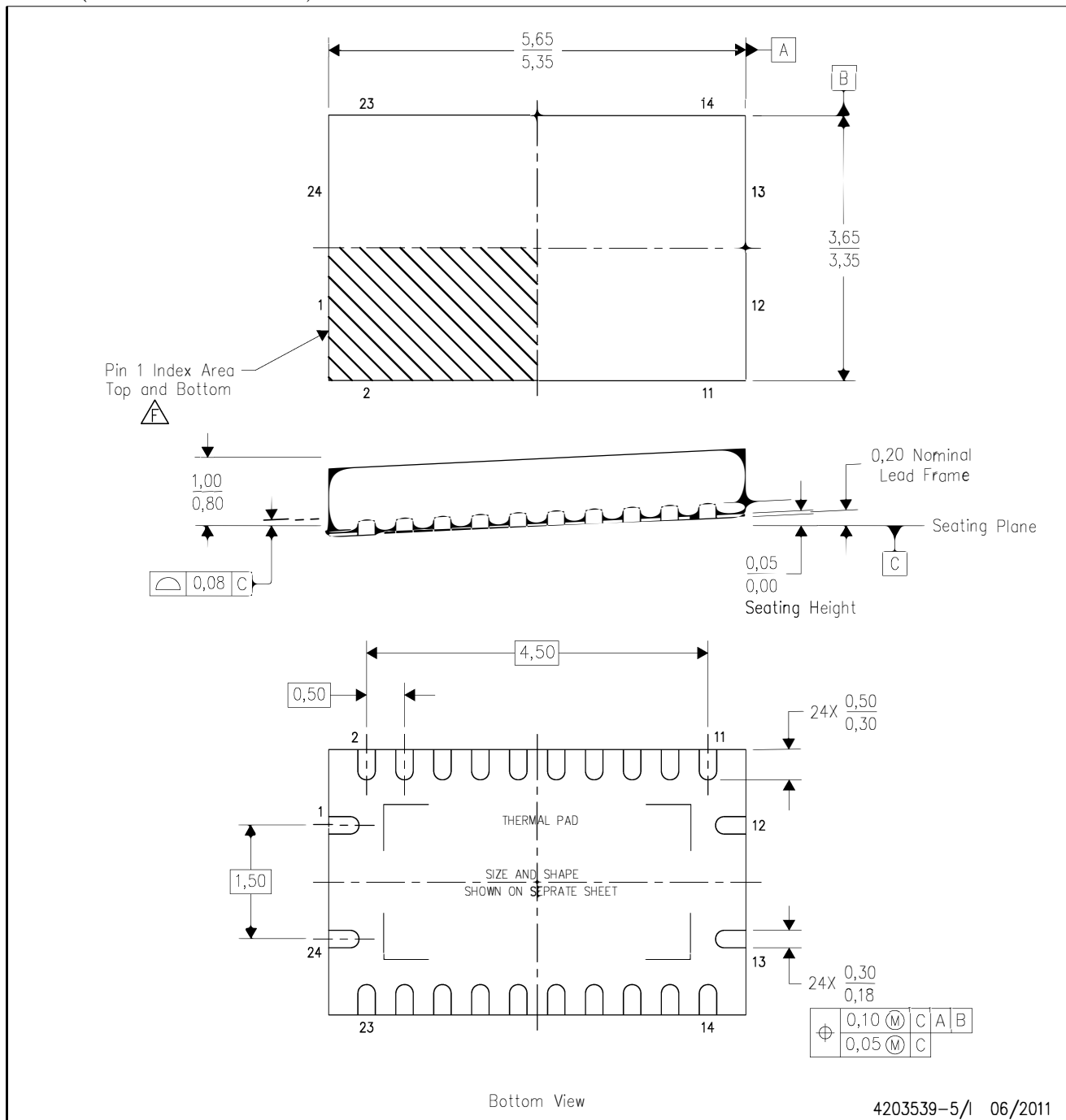


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ24171RGYR | VQFN         | RGY             | 24   | 3000 | 367.0       | 367.0      | 35.0        |
| BQ24171RGYT | VQFN         | RGY             | 24   | 250  | 210.0       | 185.0      | 35.0        |

RGY (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N24)

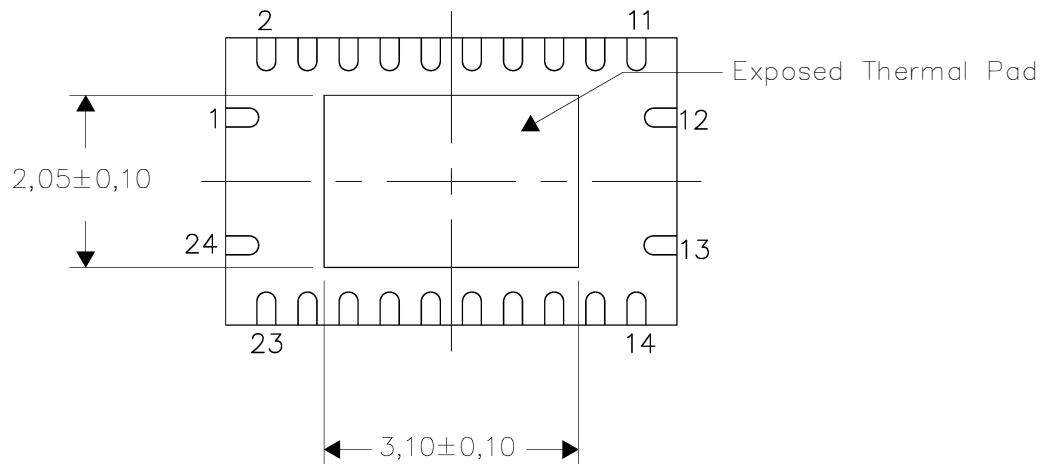
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

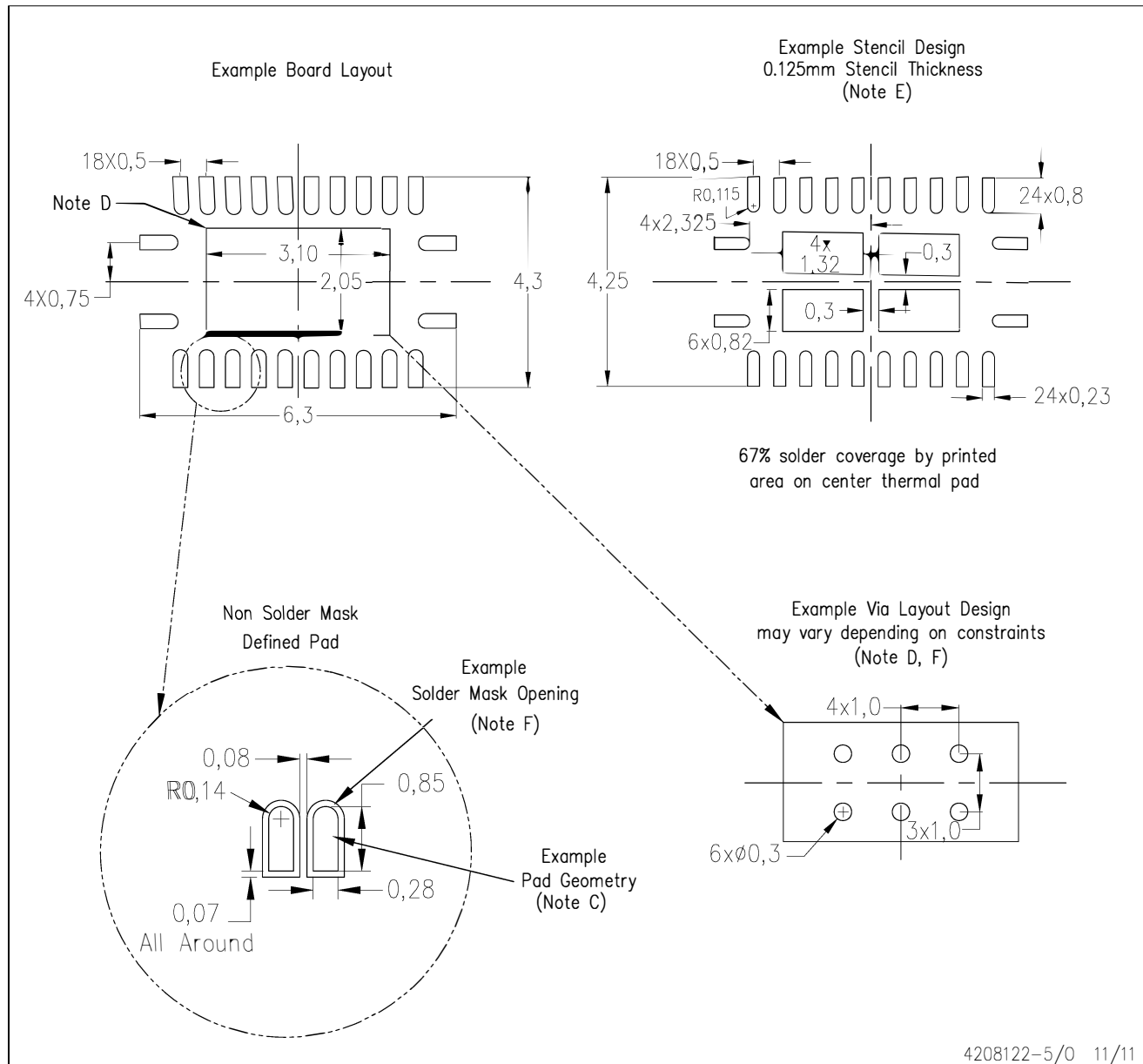
Exposed Thermal Pad Dimensions

4206353-6/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-5/0 11/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.