

3V-40V Vin, 300mA, 2.4uA I_Q, Low-Dropout Regulator with PG Feature**FEATURES**

- Wide Input Range: 3V-40V
- With up to 45V Transient Input Voltage
- Maximum Output Current : 300mA
- Output Voltage:
 - 3.3V and 5V (Fixed Output)
 - 1.2V, 1.8V, 2.5V, 3V, 4.2V and 4.5V (Need contact SCT sales)
- Output Voltage Accuracy:
 - T=25°C : ±1%
 - T= -40°C~ 125°C : ±2%
- Low Quiescent Current : 2.4uA
- Low Dropout Voltage :
 - 230mV at 100mA load current
 - 470mV at 200mA load current
- Support Output Capacitors Range:
 - 3.3uF~220uF
 - Low-ESR : 0.001Ω~ 5 Ω
- 550us Internal Soft-start Time
- Integrated Short-Circuit Protection with OCFB (Over Current Fold-back) Feature
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Power-Good Feature is available
- Over-Temperature Protection
- Available Package:
 - TSOT23-5 / TDFN2x2-6 / eMSOP3x3-8

APPLICATIONS

- Automotive Head Units
- Headlights
- Body Control Modules
- Inverter and Motor Controls

DESCRIPTION

The SCT71403 series products is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 40 V (45V transient input voltage) and 300mA output current with enable control and Power-Good feature. The SCT71403 series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended.

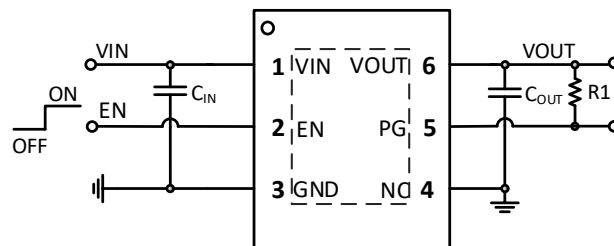
Only 2.4-μA typical quiescent current at light load makes the SCT71403 series products ideal choices for portable devices with battery power supply and an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

The SCT71403 series products implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset.

The SCT71403 series products integrated short-circuit and overcurrent protection with OCFB (Over Current Fold-back) feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71403 series products provide fixed 3.3V and 5V output voltage versions, and also could provide 1.2V, 1.8V, 2.5V, 3V, 4.2V and 4.5V fixed output voltage versions, please contact SCT sales if needed.

The SCT71403 series products is available in TSOT23-5, TDFN2x2-6 and eMSOP3x3-8 packages, for other package options, please contact SCT sales.

TYPICAL APPLICATION

SCT71403 Series

REVISION HISTORY

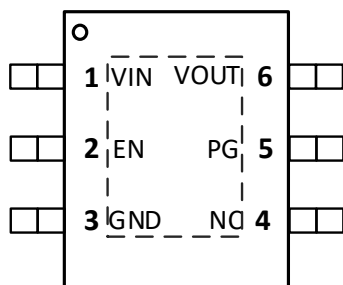
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Sampling

DEVICE ORDER INFORMATION

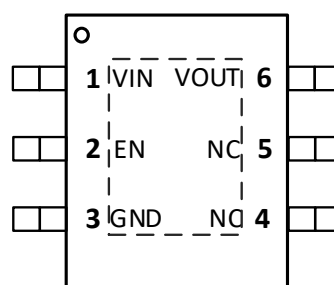
Part Number	Output Voltage	Package	Package Marking	Transport Media, Quantity
SCT71403F50A-DVAR	Fixed 5.0V	TDFN2X2-6	71403A	Tape & Reel, 3000
SCT71403F33A-DVAR	Fixed 3.3V	TDFN2X2-6	71403A	Tape & Reel, 3000
SCT71403F50-DVAR	Fixed 5.0V	TDFN2X2-6	71403	Tape & Reel, 3000
SCT71403F33-DVAR	Fixed 3.3V	TDFN2X2-6	71403	Tape & Reel, 3000
SCT71403F50-MTER	Fixed 5.0V	eMSOP3x3-8	71403	Tape & Reel, 4000
SCT71403F33-MTER	Fixed 3.3V	eMSOP3x3-8	71403	Tape & Reel, 4000
SCT71403F50-TWBR	Fixed 5.0V	TSOT23-5	71403	Tape & Reel, 3000
SCT71403F33-TWBR	Fixed 3.3V	TSOT23-5	71403	Tape & Reel, 3000

PIN CONFIGURATION



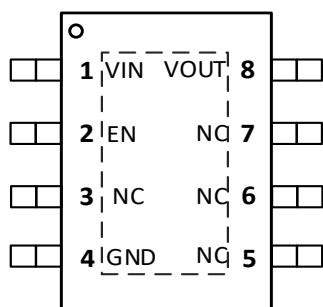
SCT71403FxxA-DVAR

TDFN2x2-6 Package



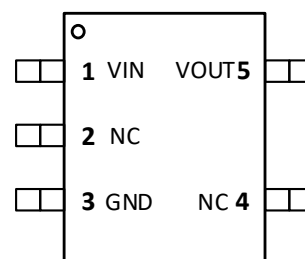
SCT71403Fxx-DVAR

TDFN2x2-6 Package



SCT71403Fxx-MTER

eMSOP3x3-8 Package



SCT71403Fxx-TWBR

TSOT23-5 Package

PIN FUNCTIONS

NAME	PIN NUMBER				PIN FUNCTION
	TDFN2x2-6-A	TDFN2x2-6	eMSOP3x3-8	TSOT23-5	
VIN	1	1	1	1	Input voltage pin
EN	2	2	2	--	Enable input pin
GND	3	3	4	3	Ground reference pin.
NC	4	4,5	3,5,6,7	2,4	No connection
PG	5	--	--	--	Power-good pin
VOUT	6	6	8	5	Regulated output voltage pin
Thermal Pad	7	7	9	--	Connect the thermal pad to a large area GND plane for improved the thermal performance.

SCT71403 Series

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Input voltage range	3	40	V
V _{OUT}	Output voltage range	1.2	5	V
V _{EN}	Enable input voltage	0	V _{IN}	V
V _{PG}	Power-good pin voltage	0	5	V
C _{IN}	Input capacitor	2.2	--	uF
C _{OUT}	Output capacitor	3.3	220	uF
ESR	Output capacitor ESR requirements	0.001	5	Ω
T _A	Operating ambient temperature	-40	125	°C
T _J	Operating junction temperature	-40	150	°C

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Maximum input voltage range	-0.3	45	V
V _{OUT}	Maximum output voltage range	-0.3	5.5	V
V _{EN}	Maximum enable input voltage	-0.3	V _{IN}	V
V _{PG}	Maximum power-good pin voltage	-0.3	5.5	V
T _J ⁽²⁾	Junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
- (2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins ⁽¹⁾	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins ⁽²⁾	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

The value of $R_{\theta JA}$ and $R_{\theta JC}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. Because they were simulated in accordance with JESD 51-7. They do not represent the performance obtained in an actual application. For design information see Power Dissipation and Thermal Performance section.

The value of $R_{\theta JA_EVM}$ and Ψ_{JT} is the tested results based on our EVM, and is more useful for thermal design. Even if they still do not represent the thermal performance of customer's PCB design, but they are a good starting point for thermal performance design.

The PCB information of our EVM : 2-layer, 1 oz Cu, 50mm x 30mm size.

The values given in this table are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB), thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the device. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual values of the below table.

Package Type	$R_{\theta JA}^{(1)}$	$R_{\theta JC}^{(2)}$	$R_{\theta JA_EVM}^{(3)}$	$\Psi_{JT}^{(4)}$	UNIT
TDFN2X2-6	TBD	TBD	62.5	TBD	°C/W
eMSOP3x3-8	TBD	TBD	TBD	TBD	
TSOT23-5	TBD	TBD	115.4	TBD	

(1) $R_{\theta JA}$ is junction to ambient thermal resistance, based on JESD51-7.

(2) $R_{\theta JC}$ is junction to case thermal resistance, based on JESD51-7.

(3) $R_{\theta JA_EVM}$ is junction to ambient thermal resistance, which is tested on SCT EVM.

(4) Ψ_{JT} is Junction-to-top characterization parameter, which is tested on SCT EVM.

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ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT}+1V$, $C_{OUT}=10\mu F$, $T_J=-40^{\circ}C\sim 125^{\circ}C$, typical value is tested under $25^{\circ}C$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3		40	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} rising	2.5	2.66	2.9	V
	Hysteresis			180		mV
I_{SHDN}	Shutdown current from V_{IN} pin	EN=0, no load, $V_{IN}=6V$		0.4		μA
		EN=0, no load, $V_{IN}=12V$		0.6		μA
I_Q	Quiescent current from GND pin	EN floating, no load, $V_{IN}=6V$		2.4		μA
		EN floating, no load, $V_{IN}=12V$		2.6		μA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	$T_J=25^{\circ}C$	-1%		1%	
		$T_J=-40^{\circ}C\sim 125^{\circ}C$	-2%		2%	
ΔV_{OUT}	Line regulation	$V_{IN}=V_{OUT}+1V$ to 40V, or $V_{IN}>3V$, $I_{OUT}=10mA$		1	10	mV
	Load regulation	$I_{OUT}=1mA$ to 300mA		10	20	mV
V_{DROP}	Dropout voltage ⁽¹⁾	$V_{IN}=V_{OUT}-0.1V$, $I_{OUT}=100mA$		230		mV
		$V_{IN}=V_{OUT}-0.1V$, $I_{OUT}=200mA$		470		mV
		$V_{IN}=V_{OUT}-0.1V$, $I_{OUT}=300mA$		730		mV
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
I_{OC}	Output current limit	V_{OUT} short to $90\% \times V_{OUT}$		500		mA
I_{SC}	Short current limit	$V_{OUT}=0V$		90		mA
$PSRR$	Power supply rejection ratio ⁽²⁾	$I_{OUT}=10mA$, $f=100Hz$, $C_{OUT}=10\mu F$		TBD		dB
		$I_{OUT}=10mA$, $f=1kHz$, $C_{OUT}=10\mu F$		TBD		dB
		$I_{OUT}=10mA$, $f=10kHz$, $C_{OUT}=10\mu F$		TBD		dB
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.23		V
V_{EN_L}	Enable low threshold			1.02		V
V_{EN_Hys}	Enable threshold hysteresis			210		mV
I_{EN_0V}	Enable pin pull-up current	EN=0V		0.35		μA
T_{SS}	Enable pin pull-up current			550		μs
Power Good						
V_{PG_R}	PG rising threshold percentage	$V_{OUT}/V_{OUT(NOM)}$, when V_{OUT} rising		91%		
V_{PG_F}	PG falling threshold percentage	$V_{OUT}/V_{OUT(NOM)}$, when V_{OUT} falling		85%		
V_{PG_LOW}	PG output low voltage	$V_{OUT}=0.8 \times V_{OUT(NOM)}$, PG sink 500 μA		44		mV
R_{PG}	PG pull down resistor	$R_{PG}=V_{PG_LOW}/0.5mA$		88		Ω
I_{PG_LKG}	PG leakage current	PG=5V, V_{OUT} in regulation		20		nA
Td_PGR	PG signal turn to high delay	From $V_{OUT}>0.91 \times V_{OUT(NOM)}$ to PG rising edge delay time		130		μs
Td_PGF	PG signal turn to low delay	From $V_{OUT}<0.85 \times V_{OUT(NOM)}$ to PG falling edge delay time		12		μs
Thermal Protection						

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T _{SD}	Thermal shutdown threshold ⁽³⁾	T _J rising		175		°C
		Hysteresis		20		°C

(1) The dropout voltage is defined as $V_{IN}-V_{OUT}$, when force V_{IN} is 100mV below the value of V_{OUT} for $V_{IN}=V_{OUT(NOM)}+1V$.

(2) PSRR is derived from bench characterization, not production test.

(3) Thermal shutdown threshold is derived from bench characterization, not production test.

TYPICAL CHARACTERISTICS

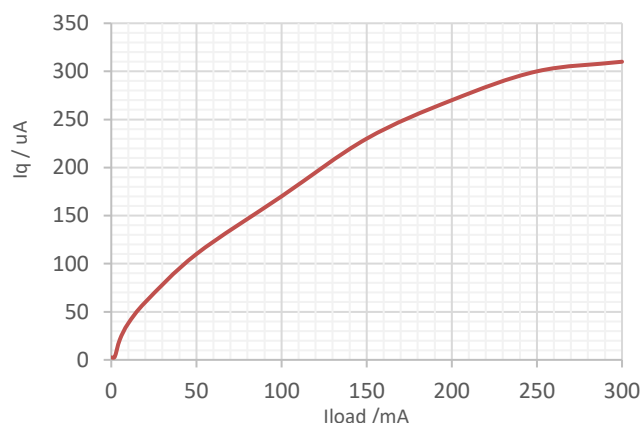


Figure 1. Quiescent Current vs Output Current

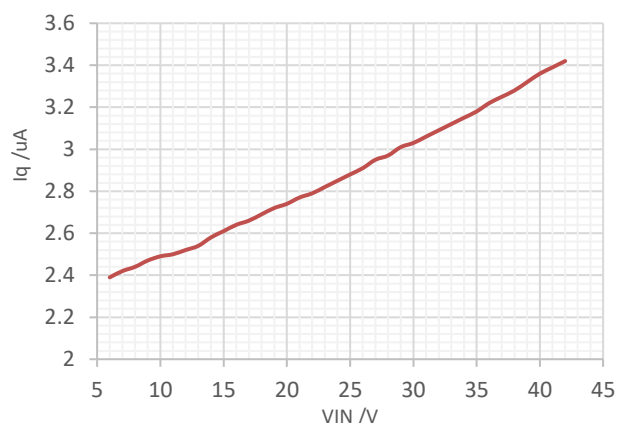


Figure 2. Quiescent Current vs Input Voltage

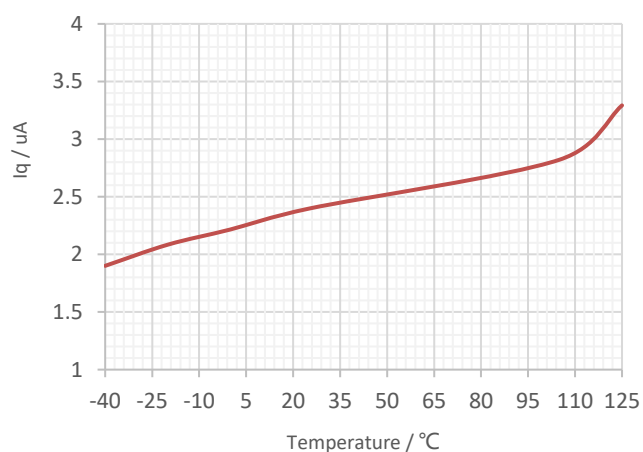


Figure 3. Quiescent Current vs Ambient Temperature

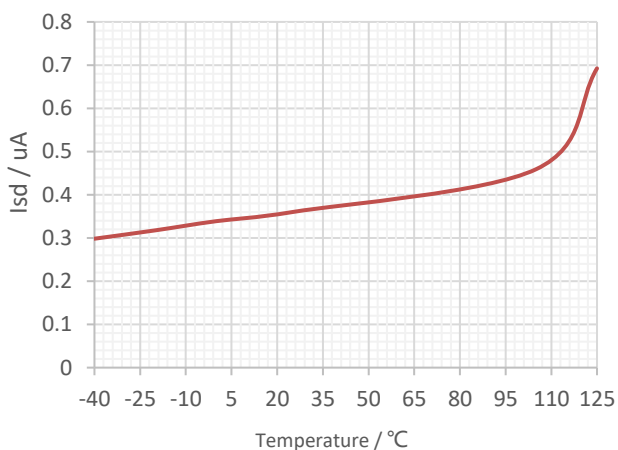


Figure 4. Shutdown Current vs Ambient Temperature

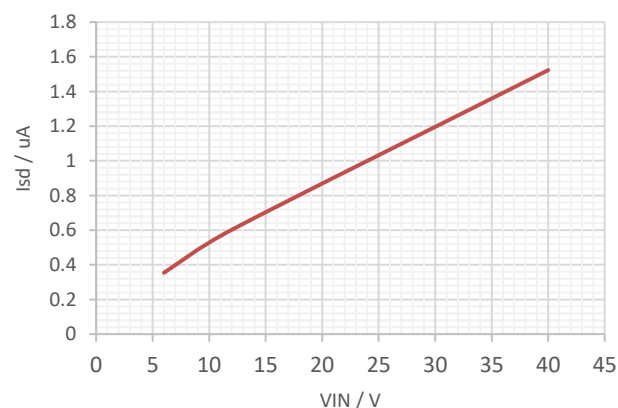


Figure 5. Shutdown Current vs Input Voltage

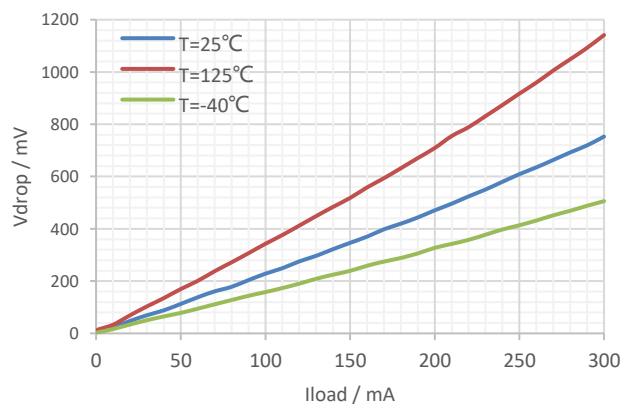


Figure 6. Dropout Voltage vs Output Current

TYPICAL CHARACTERISTICS (continued)

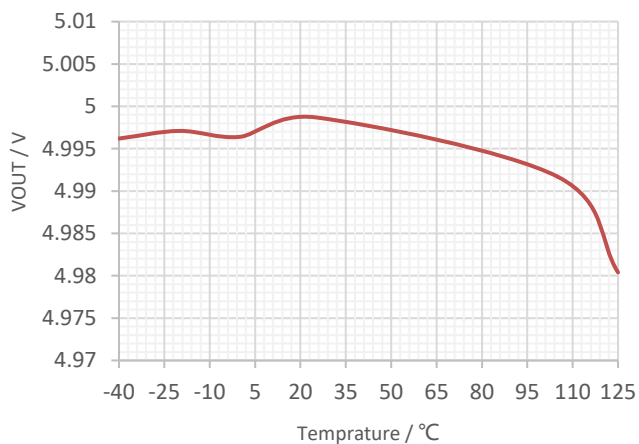


Figure 7. Output Voltage vs Ambient Temperature

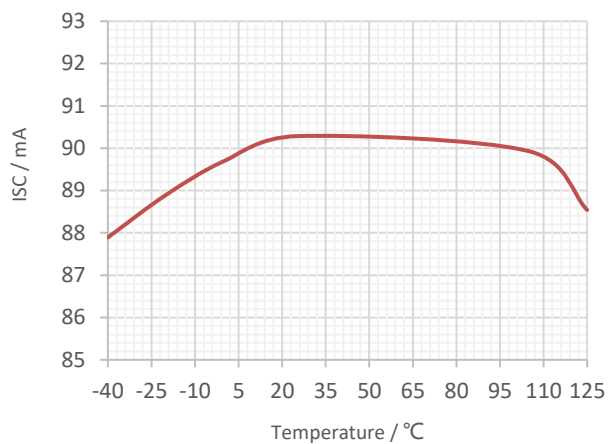


Figure 8. Short Current Limit vs Ambient Temperature

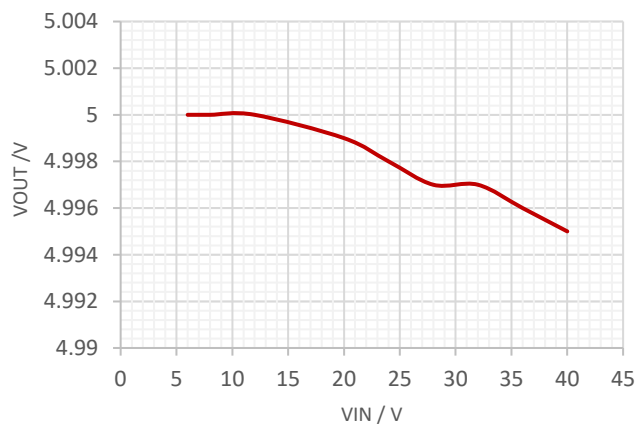


Figure 9. Output Voltage vs Input Voltage

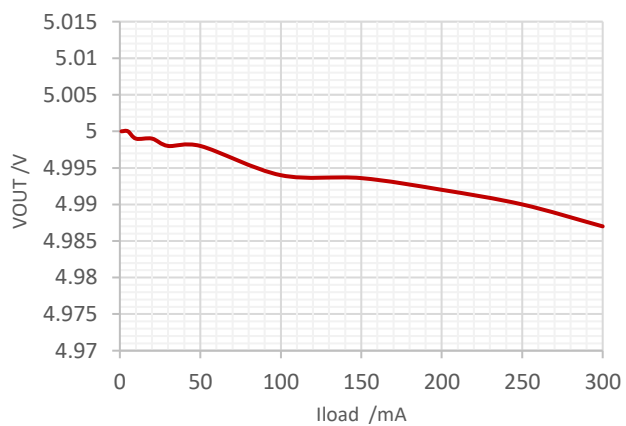


Figure 10. Output Voltage vs Output Current

FUNCTIONAL BLOCK DIAGRAM

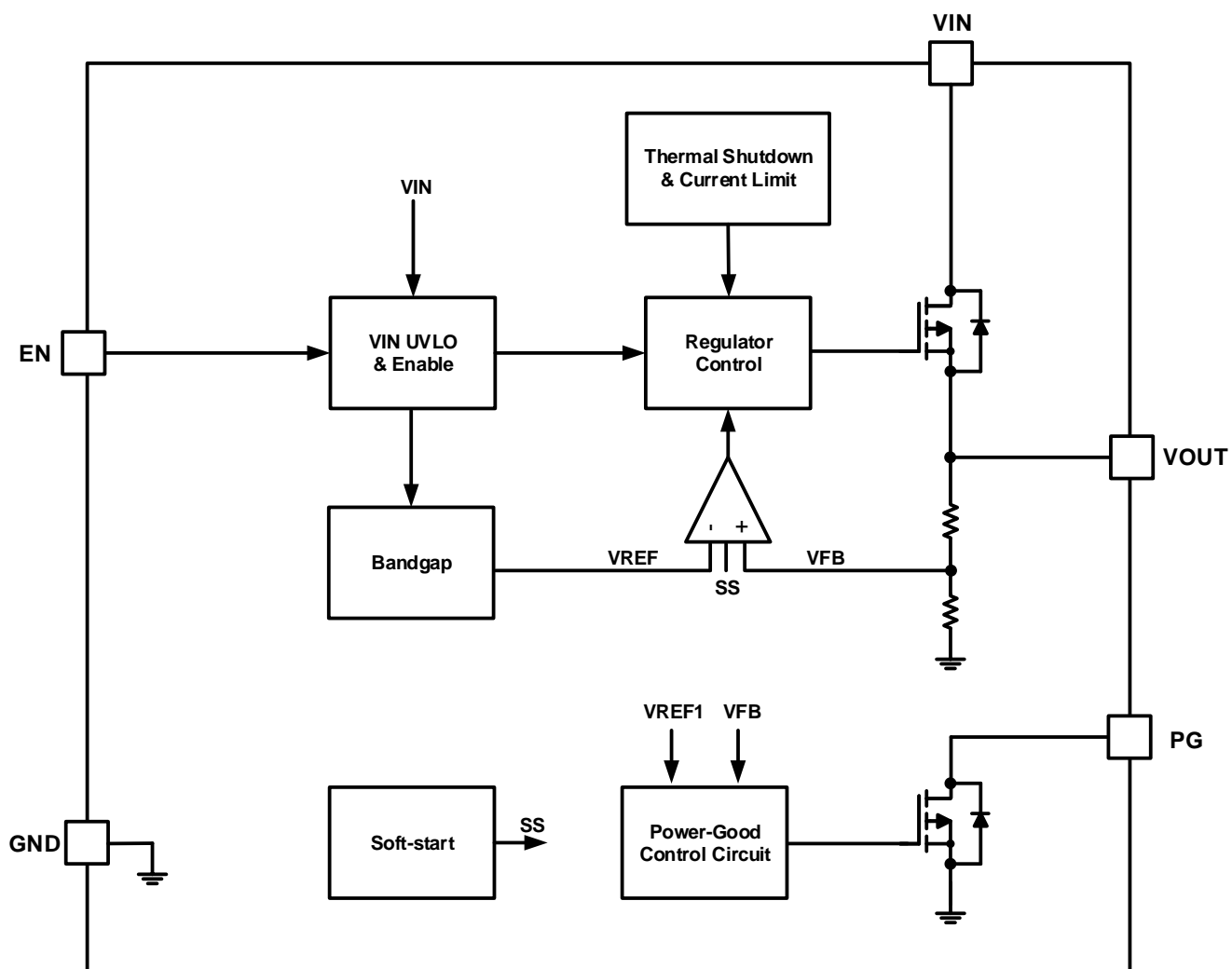


Figure 11. Functional Block Diagram

OPERATION

Overview

The SCT71403 series products are 300mA wide input voltage range linear regulators with very low quiescent current. These voltage regulators operate from 3V to 40V DC input voltage with supporting 45V transient input voltage and consume 2.4μA quiescent current at no load.

The SCT71403 series products is stable with 3.3μF~220μF output capacitors, and 10μF ceramic capacitor is recommended. An internal 550us soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71403 series products also provide enable control and Power-Good feature, which is very suitable for the applications needing sequence configuration. Other protection features include the VIN input under-voltage lockout, over current protection, output hard short protection and thermal shutdown protection.

The SCT71403 series products are available in fixed voltage versions of 3.3V and 5V with 1% output voltage accuracy at room temp and 2% output voltage accuracy over operating conditions. The series products are available in TSOT23-5, TDFN2x2-6 and eMSOP3x3-8 packages.

The SCT71403 series products also could provide other fixed output voltage versions of 1.2V, 1.8V, 2.5V, 3V, 4.2V and 4.5V and other package options of SOT23-3, TO252-5 etc. Please feel free to contact SCT sales, if you need a new output voltage version or a new package option.

Enable and Under Voltage Lockout Threshold

The SCT71403 series products is enabled when the VIN pin voltage rises above 3V and the EN pin voltage exceeds the enable threshold V_{EN_H} . The device is disabled when the VIN pin voltage falls below 2.48V or when the EN pin voltage is below V_{EN_L} . Internal pull up current source to EN pin allows the device enable when EN pin floats.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) from VIN to GND shown in Figure 9. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$VIN_{rise} = V_{EN_H} * \frac{R1 + R2}{R2} \quad (1)$$

$$VIN_{hys} = (V_{EN_H} - V_{EN_L}) * \frac{R1 + R2}{R2} \quad (2)$$

Where

VIN_{rise} : Vin rise threshold to enable the device

VIN_{hys} : Vin hysteresis threshold

$I_1=0.34\mu A$ and could be neglected in the calculation

$V_{EN_H}=1.23V$

$V_{EN_L}=1.02V$

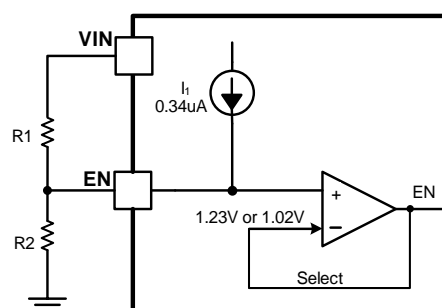


Figure 12. System UVLO by enable divide

Regulated Output Voltage

The SCT71403 series are available in fixed voltage versions of 3.3V and 5V. When the input voltage is higher than $V_{OUT(NOM)} + V_{DROPOUT}$, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)} + V_{DROPOUT}$, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

The SCT71403 series products also could provide other fixed output voltage versions of 1.2V, 1.8V, 2.5V, 3V, 4.2V and 4.5V and other package options of SOT23-3, TO252-5 etc. Please feel free to contact SCT sales, if you need a new output voltage version or a new package option.

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Over Current Limit and Foldback Current Limit

The SCT71403 series products has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{OC}). When the output voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current limit. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{OC} and I_{SC} are listed in the Electrical Characteristics table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN}-V_{OUT}) \times I_{OC}]$. When the output is shorted and the output voltage is less than $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN}-V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

The foldback voltage ($V_{FOLDBACK}$) of SCT71403 series products was set to $[50\% \times V_{OUT(NOM)}]$, when V_{OUT} falling during over current faults or shorting events. And it will recovery to brick-wall scheme from a foldback current limit scheme when the output voltage rises up to $[56\% \times V_{OUT(NOM)}]$, when over current faults or short events disappear.

With the over current foldback limit feature, the SCT71403 series products would be more robust and safer when over current faults and shorting events occur. But it also requires the maximum loading current should be smaller than I_{SC} during startup and $V_{OUT} < [56\% \times V_{OUT(NOM)}]$, once $V_{OUT} > [56\% \times V_{OUT(NOM)}]$, it will be not limited by I_{SC} any more. The characteristic is shown in the following figure.

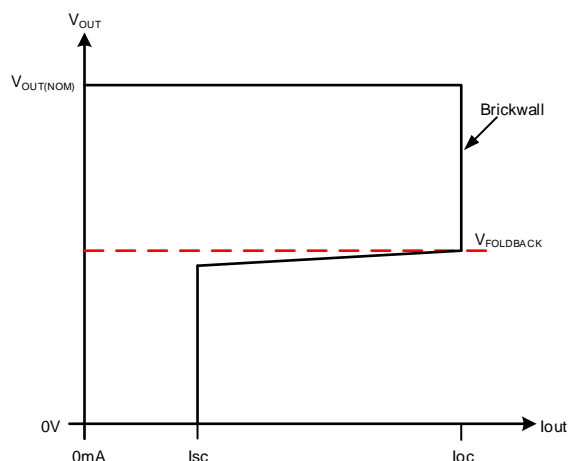


Figure 13. Current Limit with Foldback Feature

Internal Soft-Start

The SCT71403 series products integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 550 μ s. If the EN pin is pulled below 1.02V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10 μ F, the slope of V_{OUT} is limit by soft-start. When output capacitor is large, for example 100 μ F, the slope of V_{OUT} is limited by foldback current limit (I_{SC}) at $V_{OUT} < V_{FOLDBACK}$, and the slope of V_{OUT} is limited by over current limit (I_{OC}), when $V_{OUT} > V_{FOLDBACK}$.

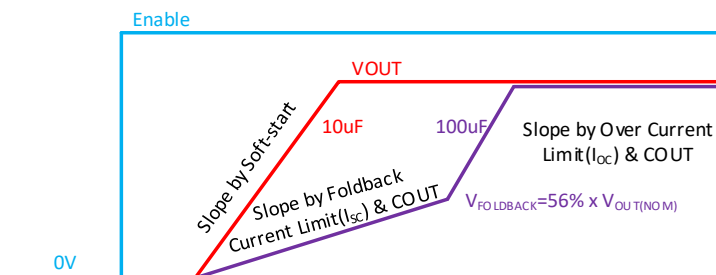


Figure 14. Soft-start Waveform vs Output Capacitor

Power-Good and Power-Good Delay

The power-good (PG) pin is an open-drain output and can be connected to any 5V or lower rail through an external pull-up resistor. And it also could be allowed to connect to power rail higher than 5V, because of integrating a zener diode from PG pin to GND internally, and in this condition, the maximum high level voltage of PG will be clamped as the breakdown voltage of zener diode, which is 5.6V typically. The PG output is high-impedance when VOUT is greater than the PG trip threshold ($V_{PG_R} = 91\% \times V_{OUT(NOM)}$). If VOUT drops below $V_{PG_F} = 85\% \times V_{OUT(NOM)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

The power-good delay time (T_{d_PGR}) is defined as the time period from when VOUT exceeds the PG trip threshold voltage (V_{PG_R}) to when the PG output is high. This power-good delay time is set by an internal time, which is 130us typical. The power-good deglitch time (T_{d_PGF}) is defined as the time period from when VOUT fall below the PG trip threshold voltage (V_{PG_F}) to when the PG output is low. This power-good deglitch time is set by an internal time, which is 12us typical. If the power-good delay time is not enough for some application, could try to connect a capacitor from PG pin to GND and using PG pull-up resistor and this capacitor generate extra delay time to meet your design.

To ensure proper operation of the power-good feature, maintain $V_{IN} \geq 3V$ (V_{IN_MIN}). It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO's VOUT level. Below are the connections examples.

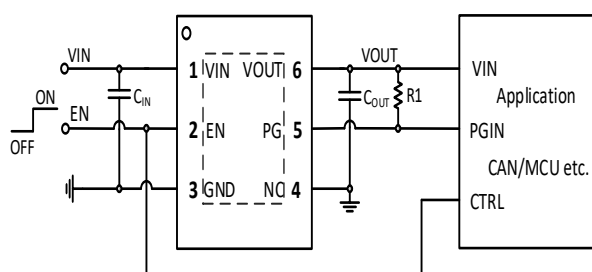


Figure 15. PG Connected to LDO's Output

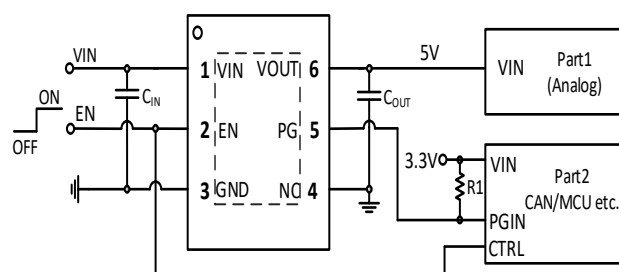


Figure 16. PG Connected to the other Power Supply

Below figure shows the startup and shutdown situation when slow power up and power down.

At the point 0, the input voltage starts to rise from 0 to 6 V, LDO is in shutdown (because VIN is below its UVLO threshold) and output voltage is 0V.

At the point 1, the VIN voltage reaches UVLO threshold level and LDO starts charging of output capacitor. VOUT rising speed is defined by internal soft-start function.

At the point 2, the VOUT voltage reaches almost the VIN voltage as it rises faster and LDO gets into dropout region. The difference between VIN and VOUT is the dropout voltage.

At the point 3, the VOUT reaches PG threshold ($V_{PG_R} = 91\% \times V_{OUT(NOM)}$) and from this point LDO counts the power good delay time (T_{d_PGR}). After this delay, the PG pin rises to high level showing that VOUT is ok.

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At the point 4, the VOUT reaches its nominal value (5.0V) as the VIN starts to be higher than ($V_{OUT(NOM)} + V_{DROP}$) and LDO gets into regulation region.

At the point 5, as the VIN voltage slow power down and LDO returns to dropout region again.

At the point 6, the VOUT drops below PG threshold ($V_{PG_F} = 85\% \times V_{OUT(NOM)}$) and LDO starts counting the power good deglitch time (T_{d_PGF}), which filters fast VOUT undershoots (caused for example by line/load transient responses). After this delay, the PG output is shorted to 0 V level to highlight “power fail” state.

At the point 7, the VIN voltage is lower than input voltage UVLO threshold minus UVLO hysteresis level and LDO goes into the shutdown state.

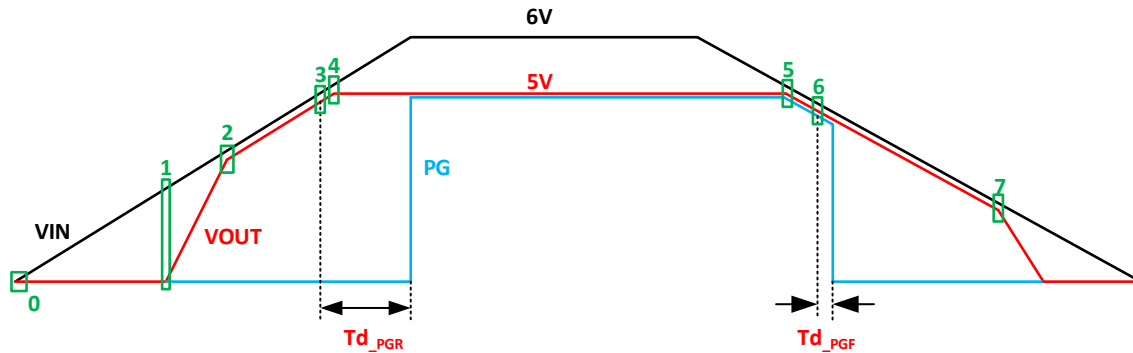


Figure 17. Startup and Shutdown Example —SCT71403 Series

Thermal Shutdown

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

APPLICATION INFORMATION

Typical application 1:

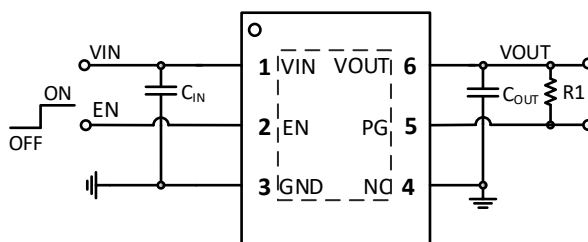


Figure 18. SCT71403 Typical Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~40V
Output Voltage	5V or 3.3V
Maximum Output Current	300mA
Output Capacitor Range (C_{OUT})	3.3uF~22uF , recommends 10uF
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF
Pull-up resistor of power-good (R1)	>10kΩ

Typical application 2:

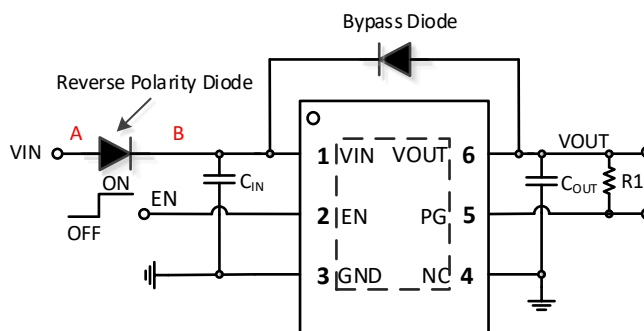


Figure 19. SCT71403 Typical Application Schematic with Reverse Polarity Diode

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~40V
Output Voltage	5V or 3.3V
Maximum Output Current	300mA
Output Capacitor Range (C_{OUT})	3.3uF~22uF , recommends 10uF
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF
Pull-up resistor of power-good (R1)	>10kΩ

SCT71403 Series

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220 μ F. Also by inserting a reverse polarity diode in series to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

Typical application 3:

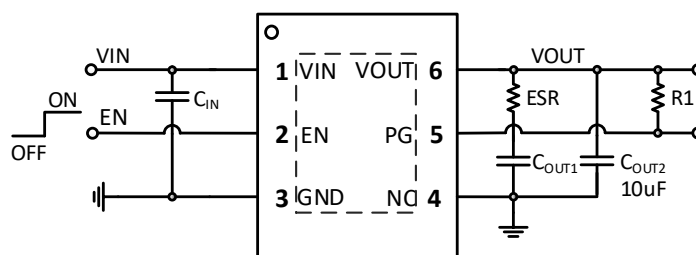


Figure 20. SCT71403 Typical Application Schematic with Large Output Capacitor

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~40V
Output Voltage	5V or 3.3V
Maximum Output Current	300mA
Output Capacitor Range (C _{OUT1} and ESR)	3.3uF~220uF with ESR=0.5 Ω ~5 Ω
Output Capacitor Range (C _{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C _{IN})	>2.2uF , recommends 10uF
Pull-up resistor of power-good (R1)	>10k Ω

Input Capacitor and Output Capacitor

SCT recommends adding a 2.2 μ F or greater capacitor with a 0.1 μ F bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage

To ensure loop stability, the SCT71403 series products requires an output capacitor with a minimum effective capacitance value of 3.3 μ F. And the series products could support output capacitor range from 3.3 μ F to 220 μ F and with an ESR range between 0.001 Ω and 5 Ω . SCT recommends selecting a X5R- or X7R-type 4.7 μ F~10 μ F ceramic capacitor with low ESR over temperature range to improve the load transient response.

When using large output capacitor with higher ESR resistor, for example 100 μ F output electrolytic capacitor with 1 Ω ESR resistor in the application, SCT recommends adding extra 10 μ F low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

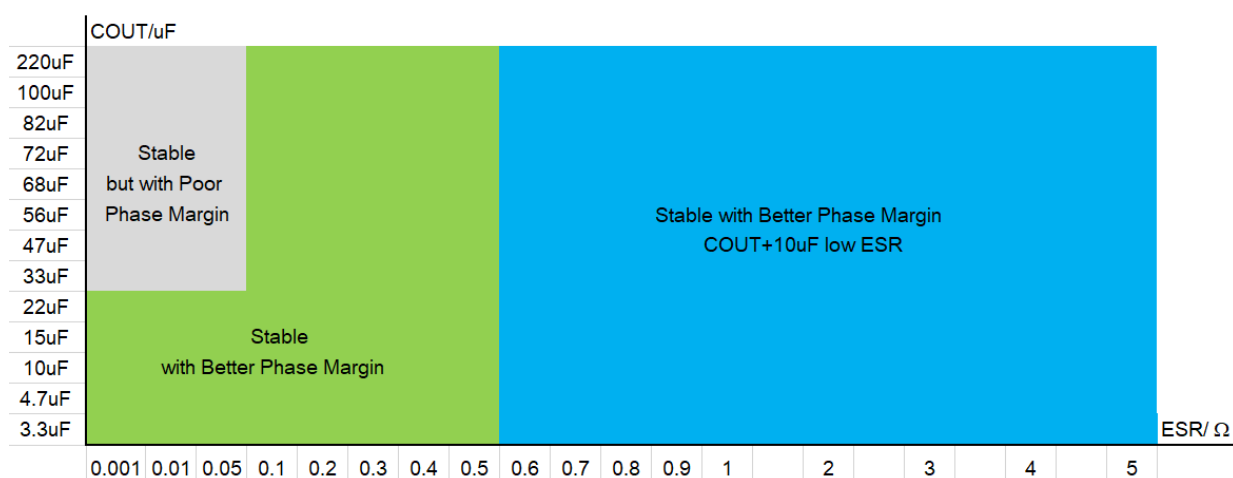


Figure 21. SCT71403 Stability vs Output Capacitor

SCT71403 Series

Power Dissipation and Thermal Performance

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3. Because $I_{GND} \ll I_{OUT}$, the term $V_{IN} \times I_{GND}$ in Equation 3 could be ignored.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. $R_{\theta JA_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J .

$$T_J = T_A + P_D \times R_{\theta JA_EVM} \quad (4)$$

$R_{\theta JA_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71403 series products, the maximum power dissipation of TDFN2x2-6 package is about 2.4W and the maximum power dissipation of TSOT23-5 package is about 1.3W based on our EVM test results, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the $R_{\theta JA_EVM}$ of TDFN2x2-6 package is 62.5 °C/W and $R_{\theta JA_EVM}$ of TSOT23-5 package is 115.4 °C/W (More accurate $R_{\theta JA_EVM}$ will be updated later, this two values are just for initial design reference, and $R_{\theta JA_EVM}$ of the eMSOP3x3-8 will be updated later). The following figures is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM : 2-layer, 1 oz Cu, 50mm x 30mm size.

Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD)	Max Allowable PD (W) ($T_J \leq 150^\circ\text{C}$)	$R_{\theta JA_EVM}$ (°C/W)
TDFN2X2-6	2.40	2.00	62.5
eMSOP3x3-8	TBD	TBD	TBD
TSOT23-5	1.30	1.08	115.4

THERMAL CHARACTERISTICS

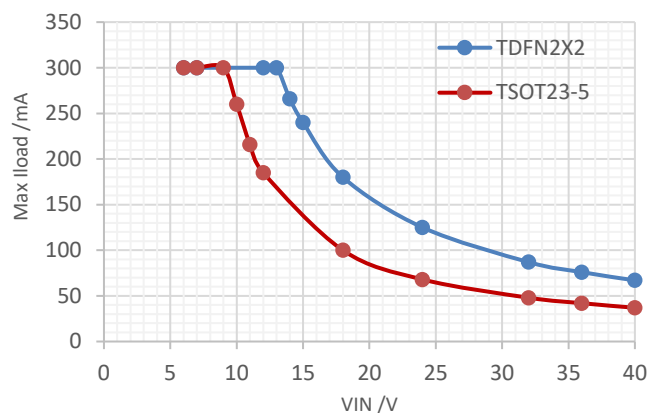


Figure 22. Maximum Output Current vs Input Voltage, TDFN2X2 and TSOT23-5, $T_J \leq T_{SD_R}$

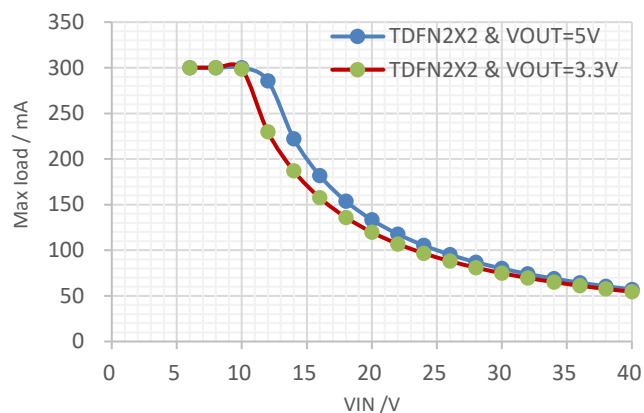


Figure 23. Maximum Output Current vs Input Voltage, TDFN2X2, $T_J \leq 150^\circ\text{C}$

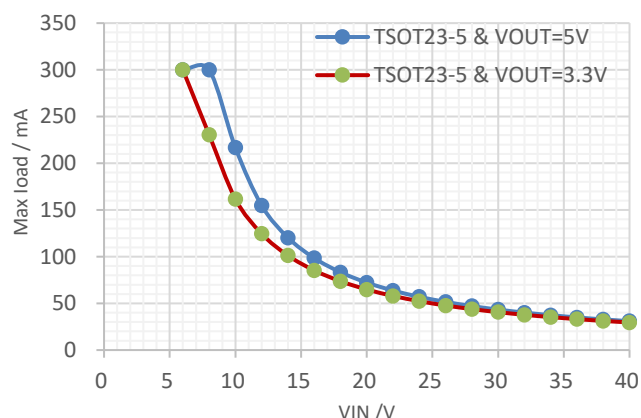


Figure 24. Maximum Output Current vs Input Voltage, TSOT23-5, $T_J \leq 150^\circ\text{C}$

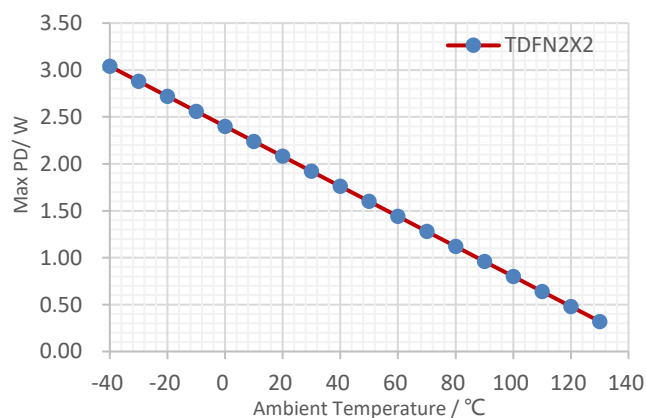


Figure 25. Maximum Allowed Power Dissipation vs Ambient Temperature, TDFN2X2, $T_J \leq 150^\circ\text{C}$

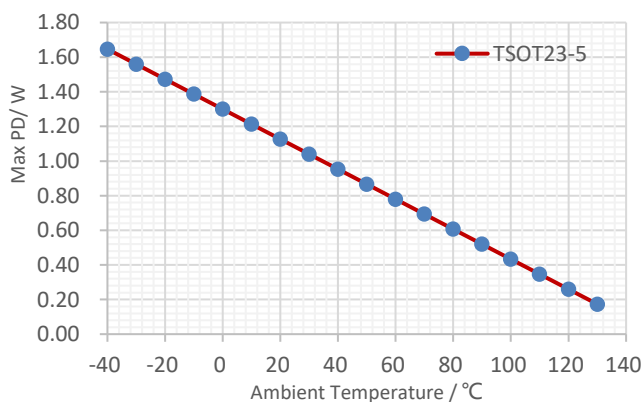


Figure 26. Maximum Allowed Power Dissipation vs Ambient Temperature, TSOT23-5, $T_J \leq 150^\circ\text{C}$

SCT71403 Series

Application Waveforms

Vin=Vout +1V, unless otherwise noted

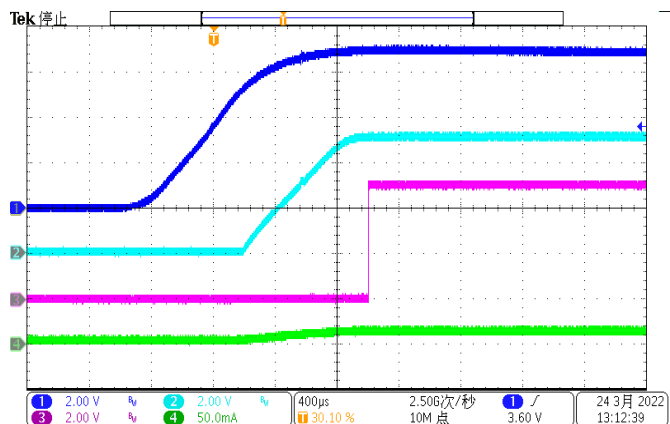


Figure 27. Power up (Iload=10mA)

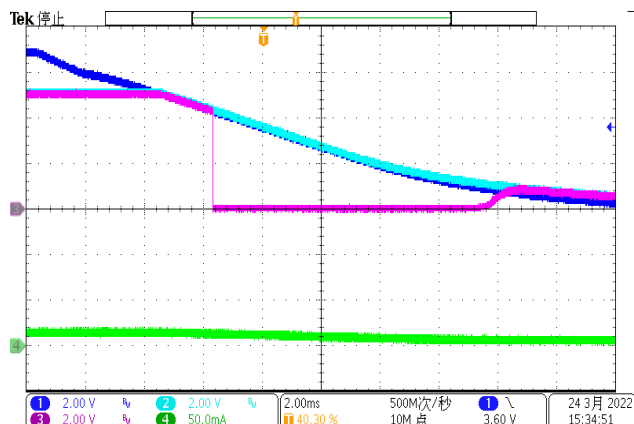


Figure 28. Power down (Iload=10mA)

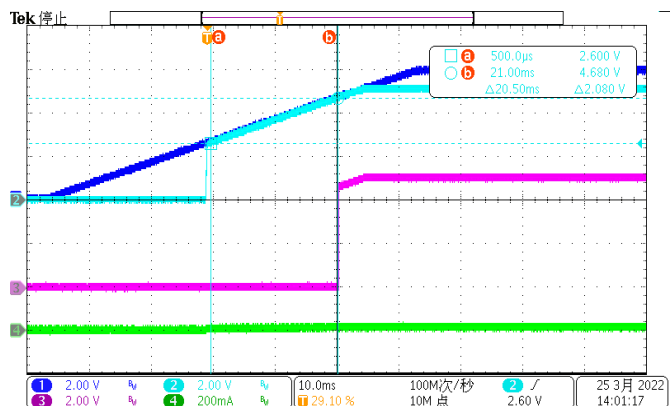


Figure 29 Slow Power up (Iload=10mA)

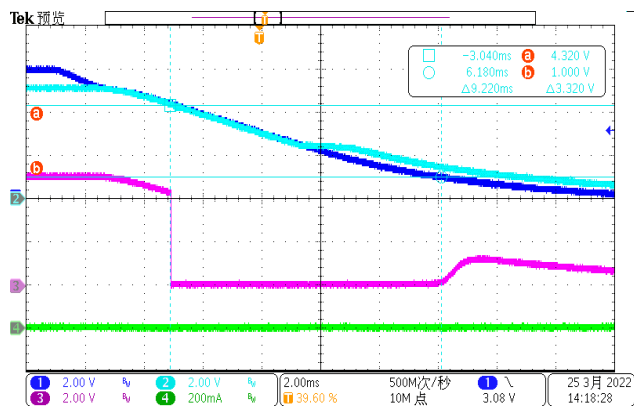


Figure 30. Slow Power down (Iload=10mA)

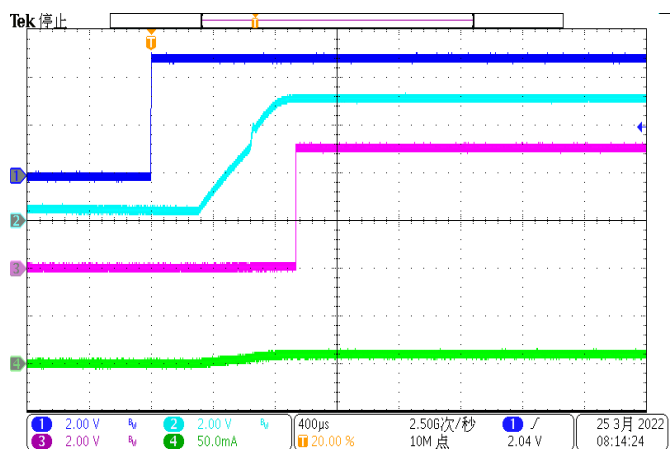


Figure 31. Enable (Iload=10mA)

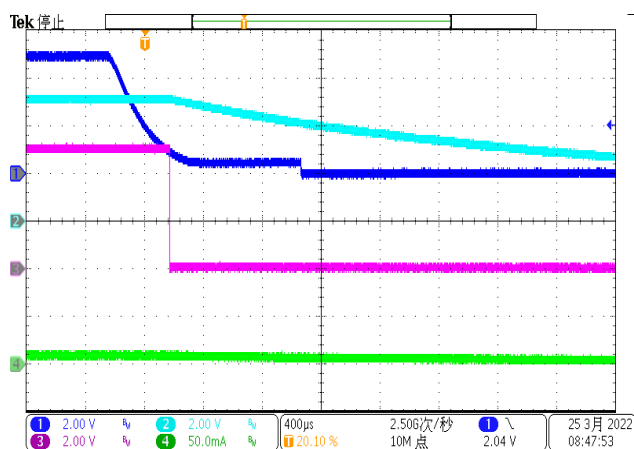


Figure 32. Disable (Iload=10mA)

Application Waveforms(Continued)

$V_{in}=V_{out}+1V$, unless otherwise noted

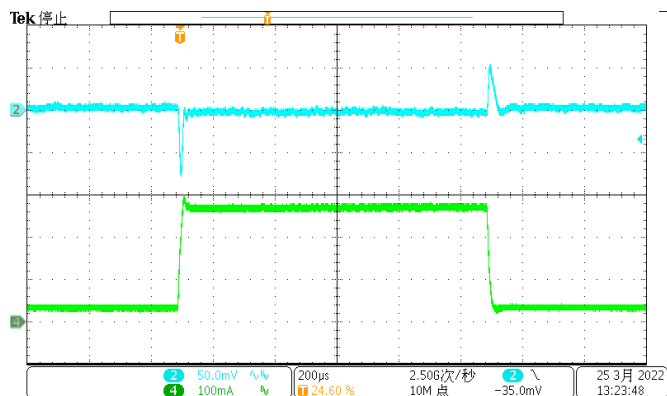


Figure 33. DC-DC Load Transient
(30mA-270mA), $V_{OUT}=5V$

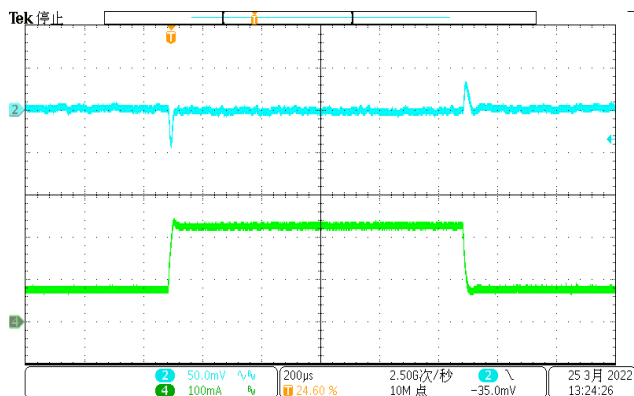


Figure 34. DC-DC Load Transient
(75mA-225mA), $V_{OUT}=5V$

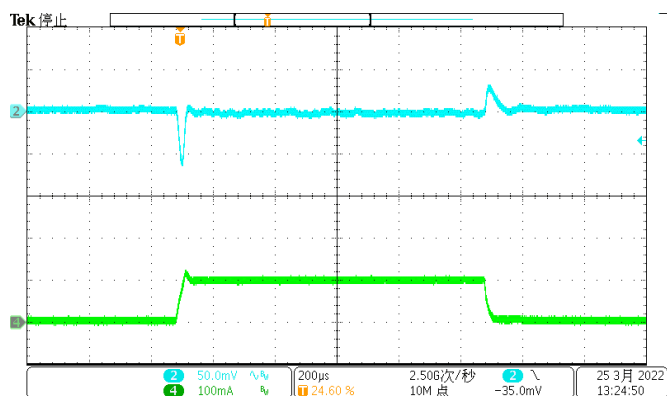


Figure 35. DC-DC Load Transient
(1mA-100mA), $V_{OUT}=5V$

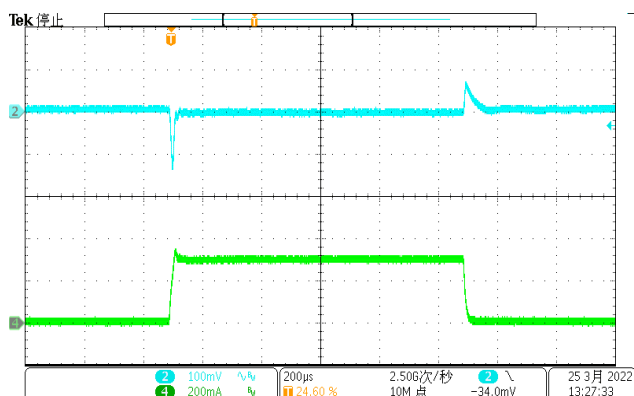


Figure 36. DC-DC Load Transient
(1mA-300mA), $V_{OUT}=5V$

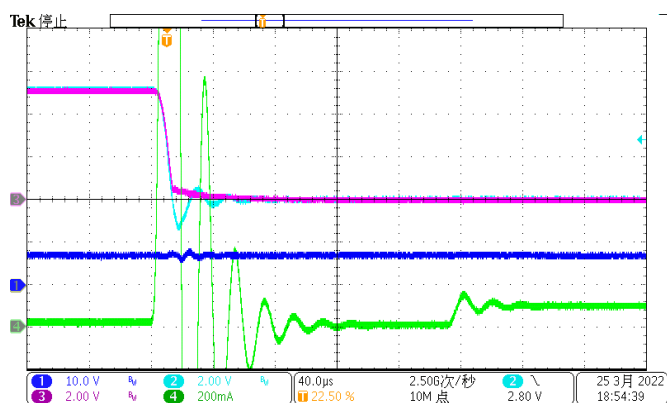


Figure 37. Enter Short Circuit Protection

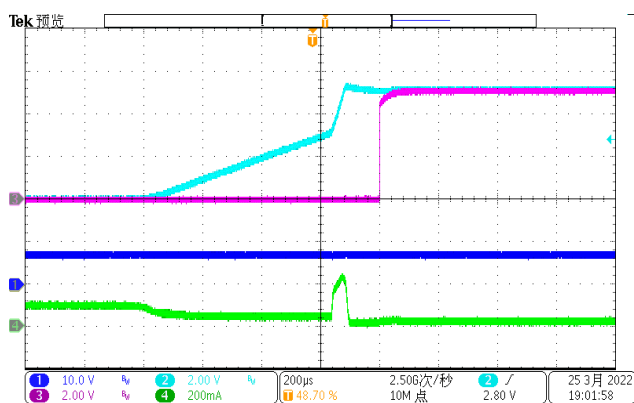


Figure 38. Exit Short Circuit Protection

SCT71403 Series

Layout Guideline

Proper PCB layout is a critical for SCT71403's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1 μ F bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize $I \times R$ drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a 10 μ F low ESR capacitor parallel connection with the large electrolytic capacitor.

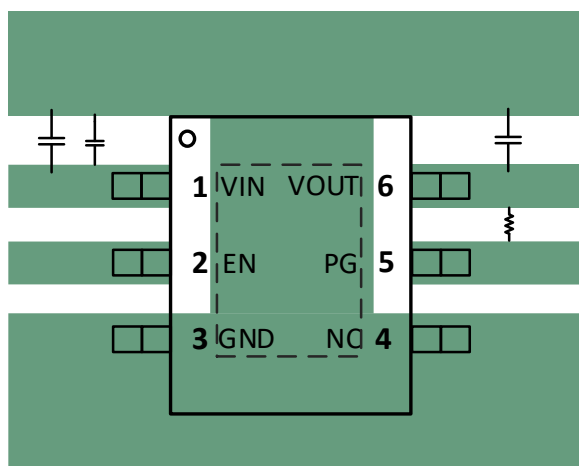


Figure 39. PCB Layout Example

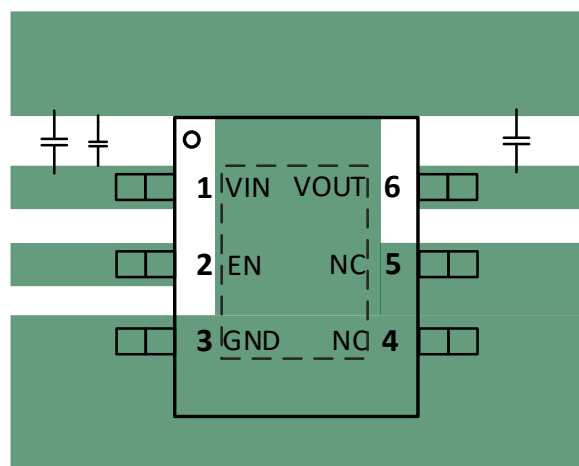


Figure 40. PCB Layout Example

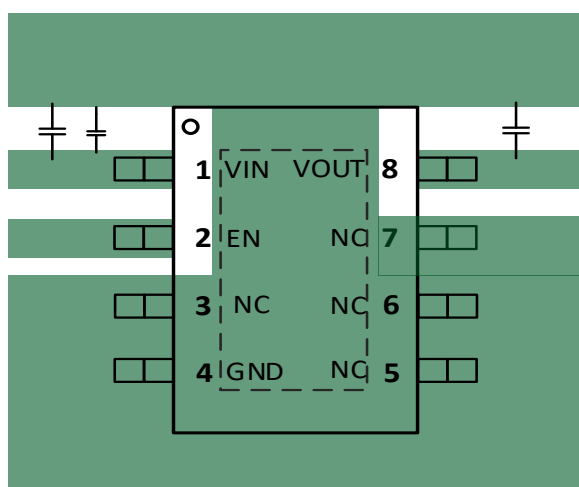


Figure 41. PCB Layout Example

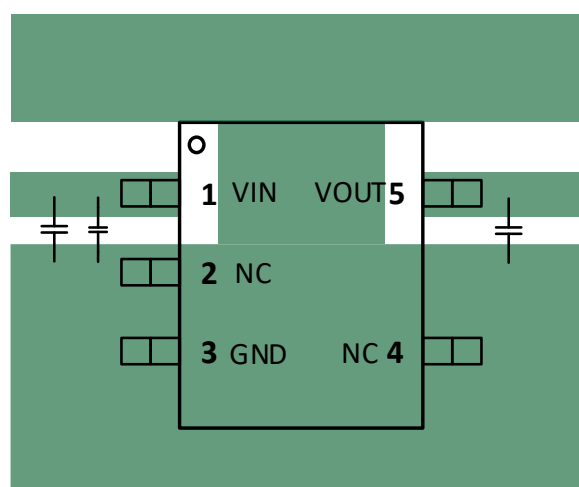
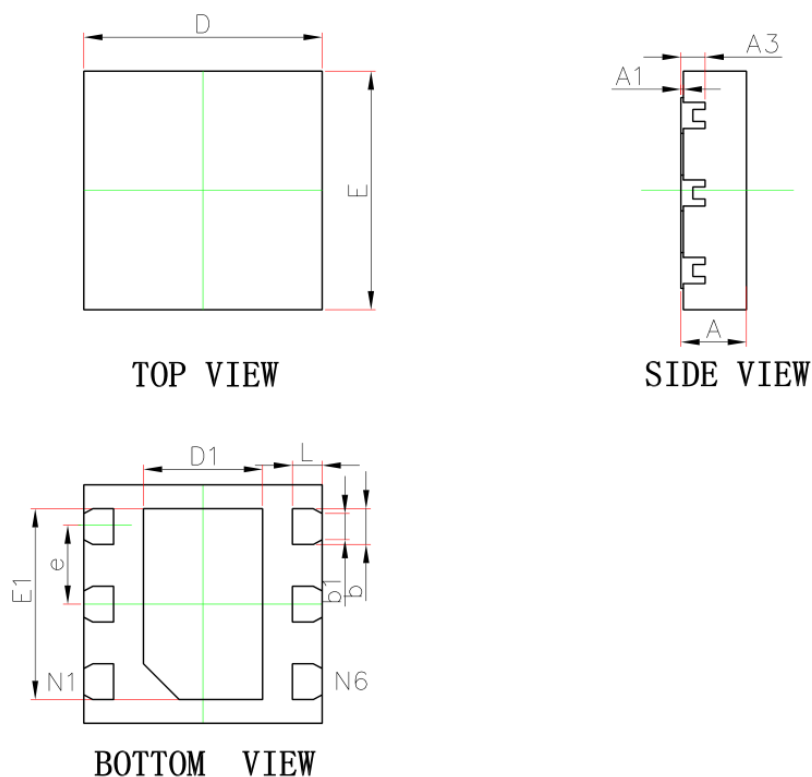


Figure 42. PCB Layout Example

PACKAGE INFORMATION



TDFN2x2-6 Package Outline Dimensions

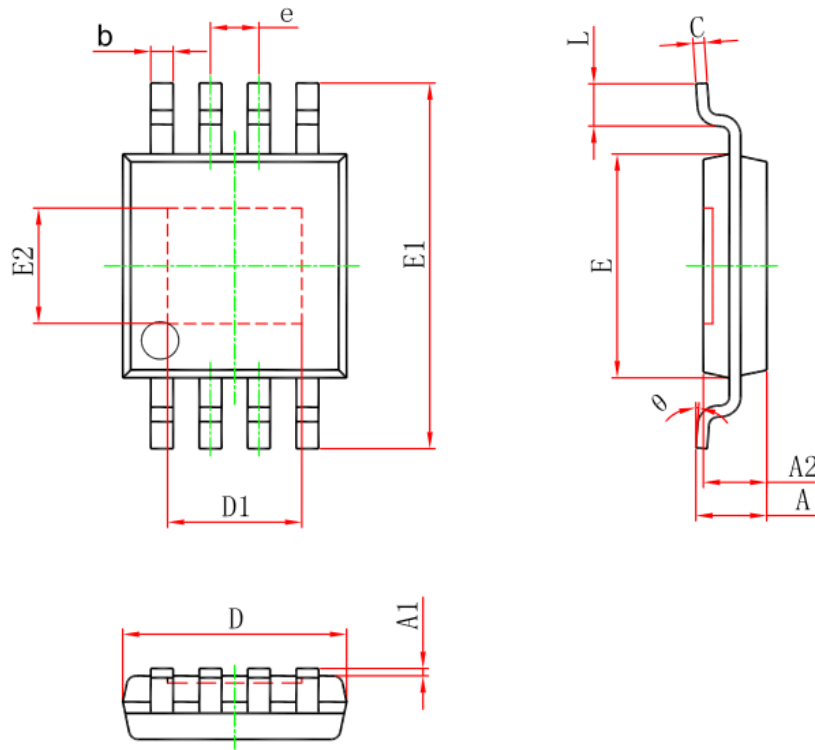
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF.		0.008 REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	1.500	1.700	0.059	0.067
b	0.250	0.350	0.010	0.014
b1	0.220 REF.		0.009 REF.	
e	0.650 BSC.		0.026 BSC.	
L	0.174	0.326	0.007	0.013

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SCT71403 Series

PACKAGE INFORMATION



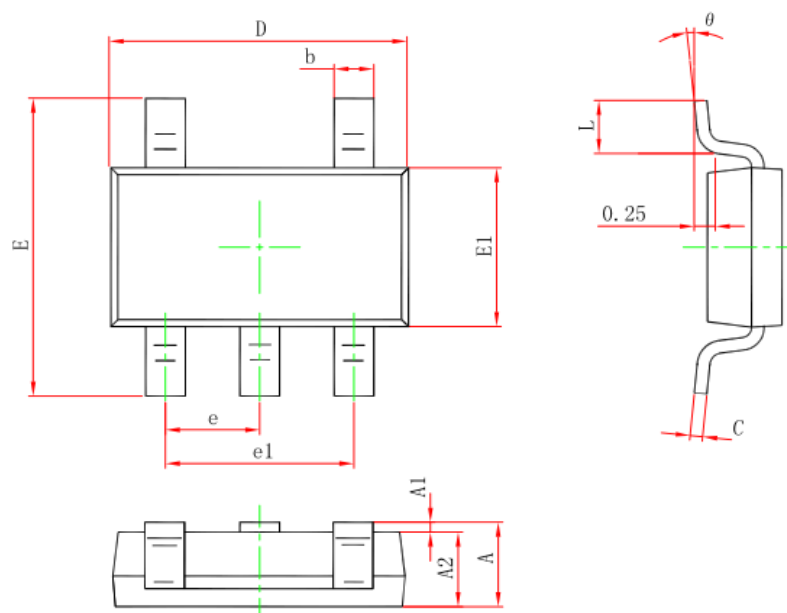
eMSOP3x3-8 Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
D1	1.700	1.900	0.067	0.075
e	0.65 (BSC)		0.026 (BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
E2	1.450	1.650	0.057	0.065
L	0.400	0.800	0.016	0.031
θ	0°	0°	0°	6°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

PACKAGE INFORMATION



TSOT23-5 Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	---	0.900	---	0.035
A1	0.020	0.090	0.001	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E1	1.600	1.700	0.063	0.067
E	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037 (BSC)	
e1	1.90 (BSC)		0.075 (BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	0°	0°	6°

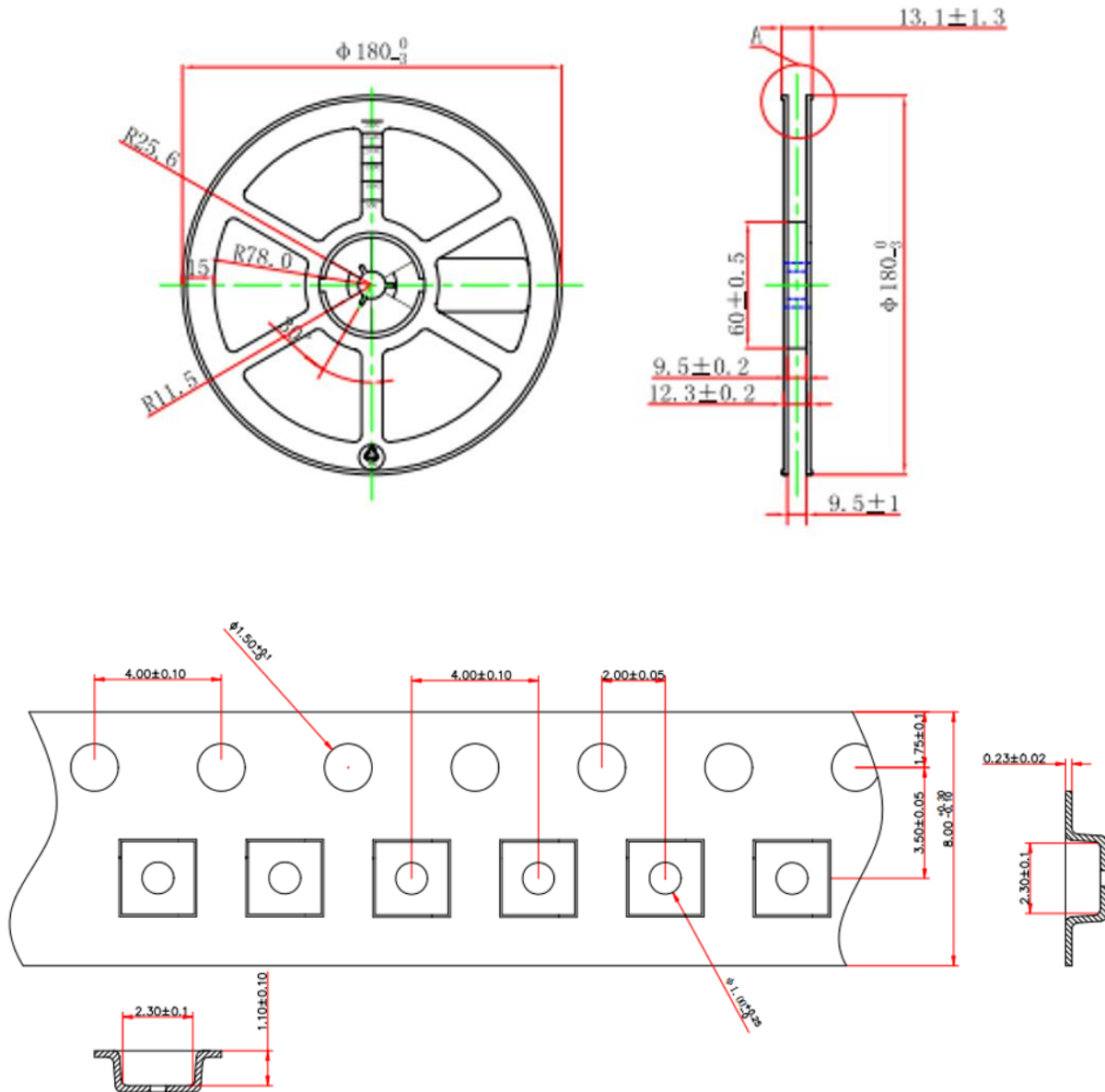
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SCT71403 Series

TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT71403 Series	TDFN2x2-6	6	3000

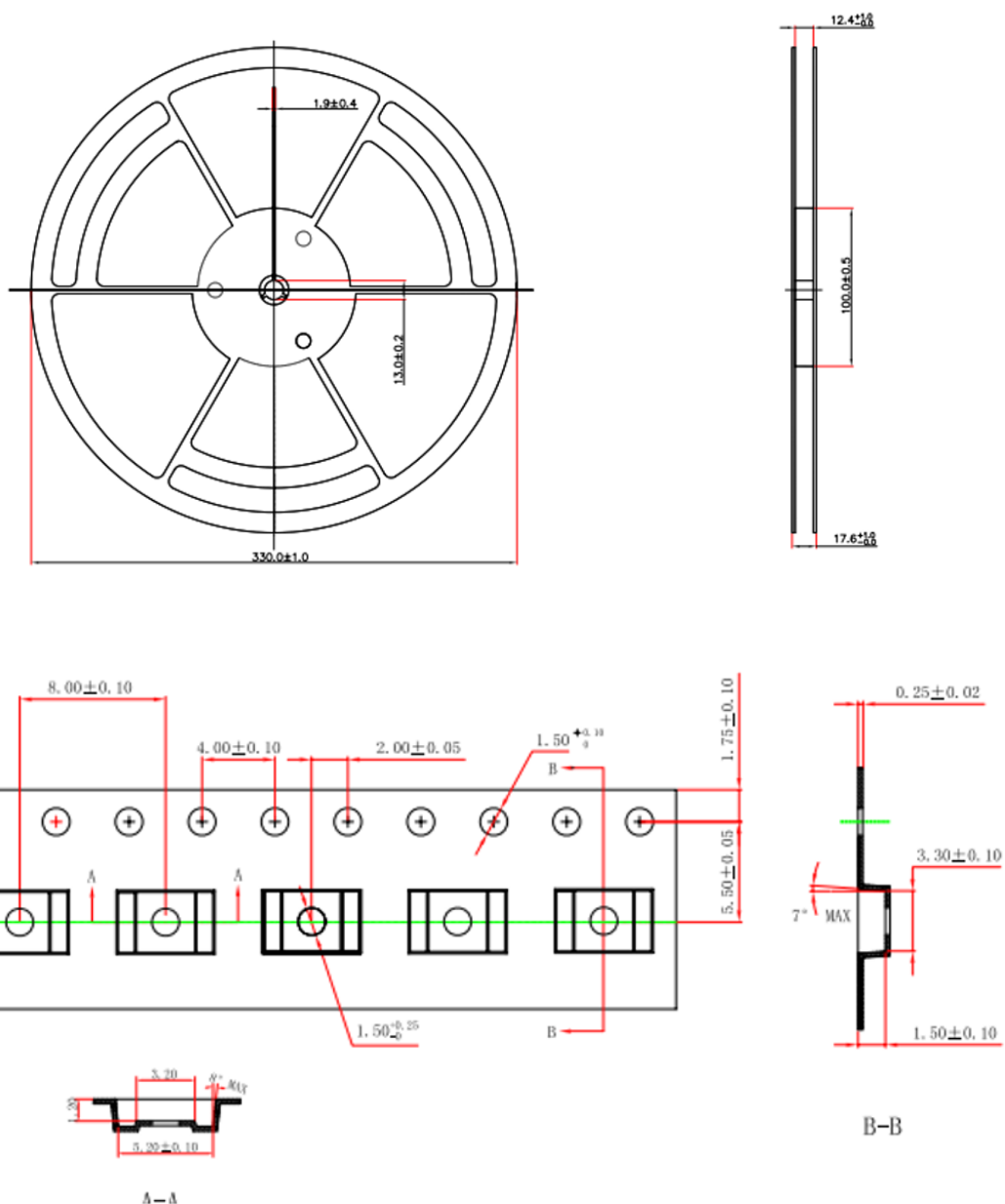


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TAPE AND REEL INFORMATION

SCT71403 Series

Orderable Device	Package Type	Pins	SPQ
SCT71403 Series	eMSOP3x3-8	8	4000

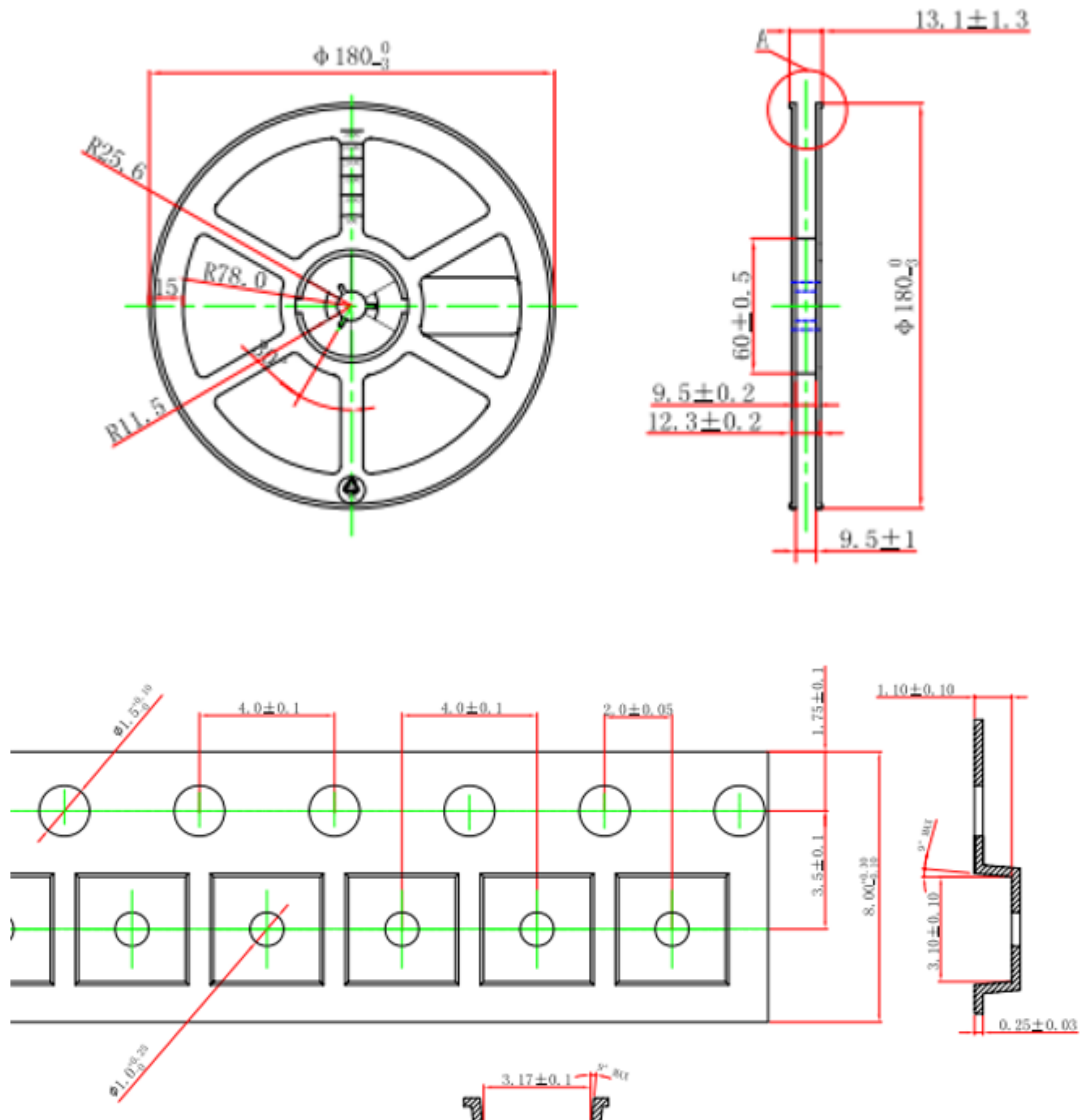


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SCT71403 Series

TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT71403 Series	TSOT23-5	5	3000



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