AOC3864

20V Common-Drain Dual N-Channel AlphaMOS

General Description

- Trench Power AlphaMOS (αMOS LV) technology
- Low $R_{SS(ON)}$
- Fully protected AlphaDFN package
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

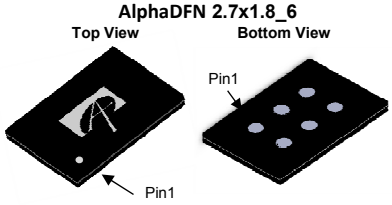
Applications

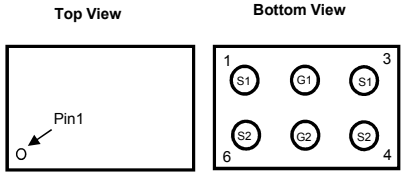
- Battery protection switch
- Mobile device battery charging and discharging

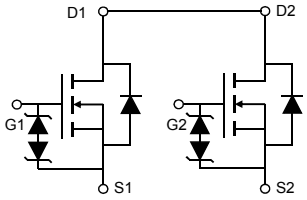
Product Summary

V_{SS}	20V
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 5.7mΩ
$R_{SS(ON)}$ (at V_{GS}=4.0V)	< 5.8mΩ
$R_{SS(ON)}$ (at V_{GS}=3.7V)	< 6mΩ
$R_{SS(ON)}$ (at V_{GS}=3.1V)	< 7.5mΩ
$R_{SS(ON)}$ (at V_{GS}=2.5V)	< 9mΩ
Typical ESD protection	**HBM Class 2**

AlphaDFN 2.7x1.8_6







Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOC3864	AlphaDFN 2.7x1.8_6	Tape & Reel	5000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Source-Source Voltage		V_{SS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Source Current(DC) Note1	T_A=25°C	I_S	19	A
Source Current(Pulse) Note2		I_{SM}	80	
Power Dissipation Note1	T_A=25°C	P_D	2.4	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typical	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	43	°C/W
Maximum Junction-to-Ambient	Steady-State		52	°C/W

Note 1. I_s rated value is based on bare silicon.Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 µs pulses, duty cycle 1% max.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{SSS}	Source-Source Breakdown Voltage	I_S=250µA, V_{GS}=0V Test Circuit 6	20			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=20V, V_{GS}=0V Test Circuit 1			1	µA
		T_J=55°C			5	
I_{GSS}	Gate leakage current	V_{SS}=0V, V_{GS}=±8V Test Circuit 2			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS}, I_S=250µA Test Circuit 3	0.5	0.9	1.3	V
$R_{SS(ON)}$	Static Source to Source On-Resistance	V_{GS}=4.5V, I_S=4A Test Circuit 4	3.4	4.5	5.7	mΩ
		T_J=125°C	4.7	6.2	7.9	
		V_{GS}=4.0V, I_S=4A Test Circuit 4	3.5	4.6	5.8	mΩ
		V_{GS}=3.7V, I_S=4A Test Circuit 4	3.6	4.7	6.0	mΩ
		V_{GS}=3.1V, I_S=4A Test Circuit 4	3.7	5.2	7.5	mΩ
		V_{GS}=2.5V, I_S=4A Test Circuit 4	3.8	5.9	9.0	mΩ
g_{FS}	Forward Transconductance	V_{SS}=5V, I_S=4A Test Circuit 3		55		S
V_{FSS}	Forward Source to Source Voltage	I_S=1A,V_{GS}=0V Test Circuit 5		0.60	1	V
DYNAMIC PARAMETERS						
R_g	Gate resistance	f=1MHz		1		KΩ
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{G1S1}=4.5V, V_{SS}=10V, I_S=4A		27	38	nC
$t_{D(on)}$	Turn-On DelayTime	V_{G1S1}=4.5V, V_{SS}=10V, R_L=2.5Ω, R_{GEN}=3Ω Test Circuit8		1.2		µs
t_r	Turn-On Rise Time			2.2		µs
$t_{D(off)}$	Turn-Off DelayTime			5.5		µs
t_f	Turn-Off Fall Time			6.5		µs

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

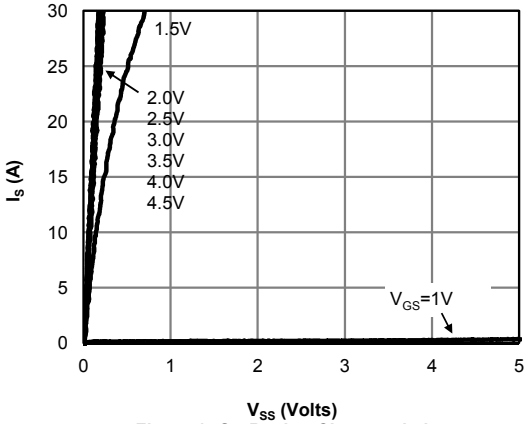


Figure 1: On-Region Characteristics

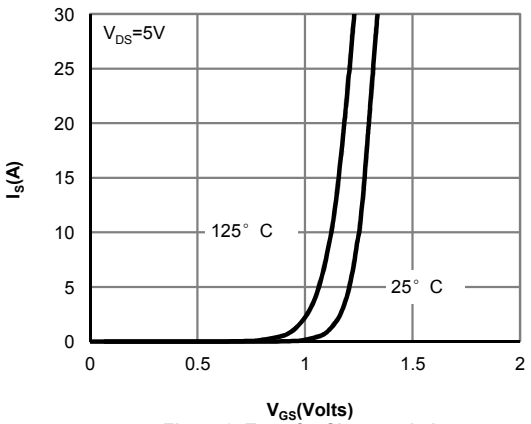


Figure 2: Transfer Characteristics

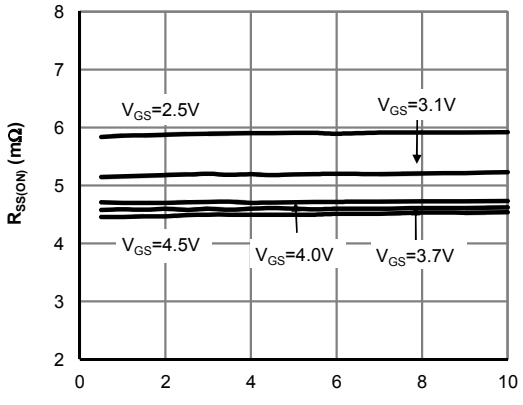


Figure 3: On-Resistance vs. Source Current and Gate Voltage

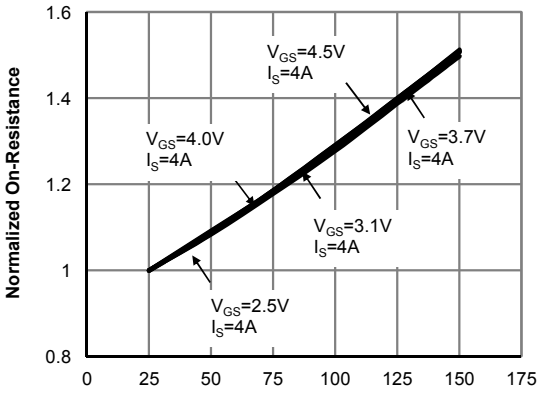


Figure 4: On-Resistance vs. Junction Temperature

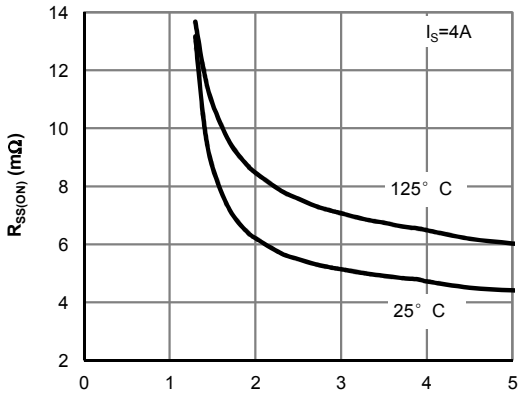


Figure 5: On-Resistance vs. Gate-Source Voltage

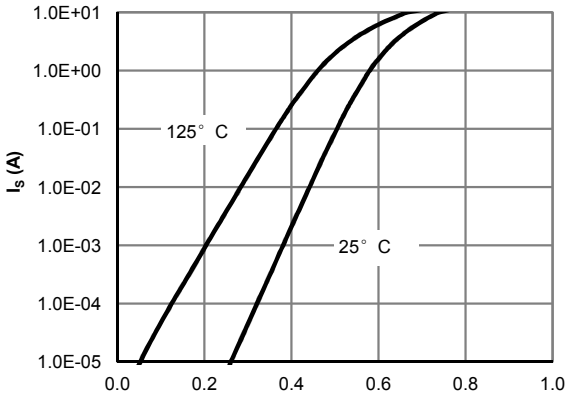


Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

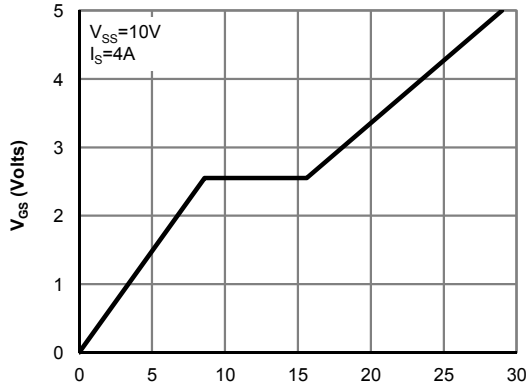


Figure 7: Gate-Charge Characteristics

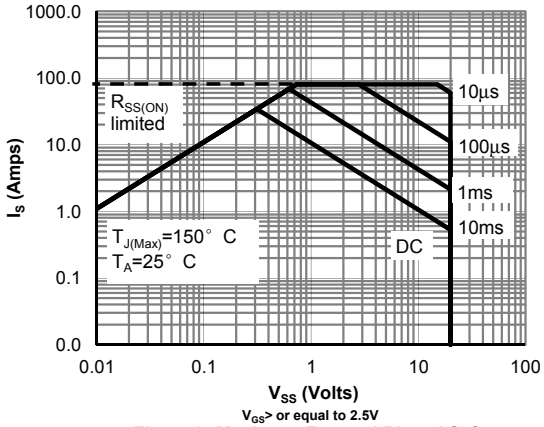


Figure 9: Maximum Forward Biased Safe Operating Area (Note1)

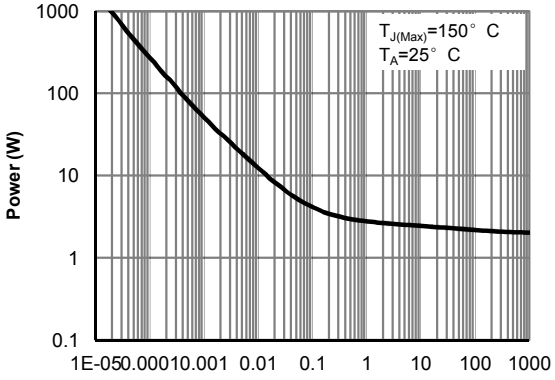


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note1)

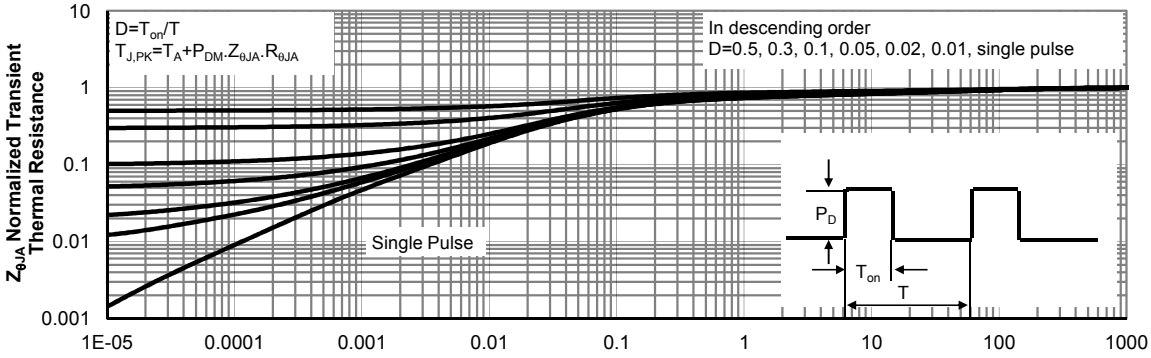
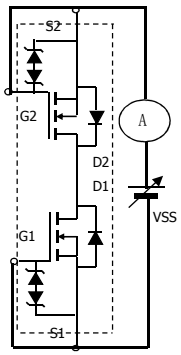


Figure 11: Normalized Maximum Transient Thermal Impedance (Note1)

TEST CIRCUIT 1 Isss

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

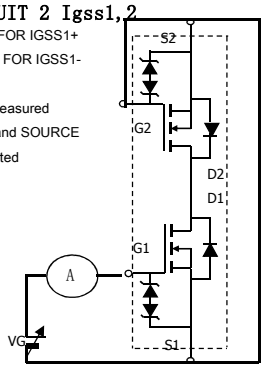


TEST CIRCUIT 2 Igss1,2

POSITIVE VGS FOR IGSS1+

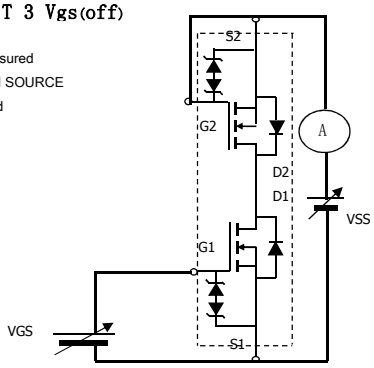
NEGATIVE VGS FOR IGSS1-

When FET1 is measured between GATE and SOURCE of FET2 are shorted



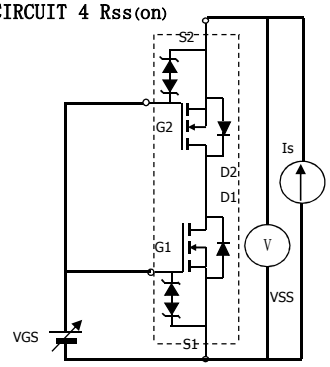
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured between GATE and SOURCE of FET2 are shorted



TEST CIRCUIT 4 Rss(on)

Vss/Is

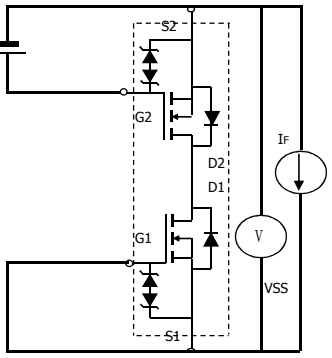


TEST CIRCUIT 5 $V_{F(SS)1,2}$

4.5V

When FET1 measured FET2 VGS=4.5V

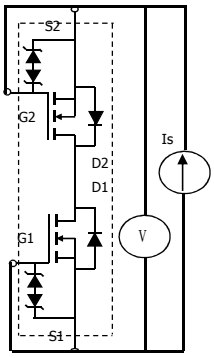
VGS=0



TEST CIRCUIT 6 BV_{DSS}

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

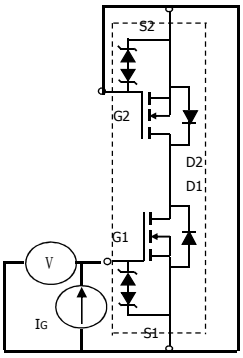


TEST CIRCUIT 7 $BV_{GSO1,2}$

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

When FET1 is measured between GATE and SOURCE of FET2 are shorted



TEST CIRCUIT 8 Switching time