# SGM5207
# 48 Channels, 12-Bit Analog Monitor and Controller with Multichannel ADC, Bipolar DACs, Temperature Sensor and GPIO Ports

## GENERAL DESCRIPTION

The SGM5207 is a high integrated analog front end, which includes 12-bit 48 channels digital-to-analog converters (DACs), a 12-bit 6 channels inputs successive approximation (SAR) analog-to-digital converter (ADC), a temperature sensor and an on-chip reference.

The chip also has 6 channels general purpose inputs and outputs (GPIOs). These pins are configurable for ADC inputs or GPIOs.

The chip is operated by a 3-wire SPI-compatible interface.

The SGM5207 is available in a Green TQFP-10×10-64L (Exposed Pad) package. It is specified from -40℃ to +125℃.

## APPLICATIONS

Active Antenna System mMIMO
Distributed Antenna Systems
Macro Remote Radio Unit
Radar
Outdoor Backhaul Unit

## FEATURES

- **48 Monotonic 12-Bit DACs**
  - **Programmable Voltage Ranges: -10V to 0V, -5V to 0V, 0V to 5V, and 0V to 10V**
  - **Support Auto-Range Detector**
- **12-Bit SAR ADC**
  - **0V to 5V and 0V to 2.5V Input Ranges**
  - **250kSPS Data Rate**
  - **Support Programmable Out-of-Range Alarms**
- **6 ADCn/GPIOn Pins: Support ADC and GPIO Configurations**
- **Support General Purpose Input/Output (GPIO)**
- **Internal Temperature Sensor**
  - **Resolution: 0.0625℃**
  - **Accuracy: ±1.5℃ (TYP)**
- **Internal 2.5V Reference**
- **Support Built-In Sequencing Features**
- **Low-Power SPI-Compatible Serial Interface**
  - **SGM5207 3-Wire Mode, 1.65V to 3.6V**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green TQFP-10×10-64L (Exposed Pad) Package**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM5207 | TQFP-10×10-64L (Exposed Pad) | -40℃ to +125℃ | SGM5207XTFF64G/TR | SGM5207<br>XTFF64<br>XXXXX | Tape and Reel, 1000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

**X XXX X**

- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

- $V_{DD}$ .......... -0.3V to 6V
- $V_{IO}$ .......... -0.3V to 6V
- $V_{CCA}$, $V_{CCB}$ .......... -0.3V to 12V
- $V_{SSA}$, $V_{SSB}$ .......... -12V to 0.3V

$V_{CCA}$ to $V_{SSA}$ .......... -0.3V to 12V

$V_{CCB}$ to $V_{SSB}$ .......... -0.3V to 12V

Pin Voltage Range (with Respect to GND)

- DAC_A[0-31] .......... $V_{SSA}$ - 0.3V to $V_{CCA}$ + 0.3V
- DAC_B[0-15] .......... $V_{SSB}$ - 0.3V to $V_{CCB}$ + 0.3V
- GPIO[0-5] .......... -0.3V to $V_{DD}$ + 0.3V
- Serial Interface Pins .......... -0.3V to $V_{IO}$ + 0.3V

ADC Analog Input Current .......... -10mA to 10mA

ADCn/GPIOn Digital Sinking Current .......... 5mA

Junction Temperature .......... +150℃

Storage Temperature Range .......... -65℃ to +150℃

Lead Temperature (Soldering, 10s) .......... +260℃

ESD Susceptibility

HBM .......... 2000V

CDM .......... 500V

## RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage Range, $V_{DD}$ .......... 4.5V to 5.5V

Digital IO Supply Voltage Range, $V_{IO}$ .......... 1.65V to 3.6V

Output Buffer Positive Supply Voltage Range, $V_{CCA}$, $V_{CCB}$ (1) .......... 4.5V to 11V

Output Buffer Negative Supply Voltage Range, $V_{SSA}$, $V_{SSB}$ (2) .......... -11V to -4.5V

Group A Output Buffer Supply Voltage Range, $V_{CCA}$ - $V_{SSA}$ .......... 4.5V to 11V

Group B Output Buffer Supply Voltage Range, $V_{CCB}$ - $V_{SSB}$ .......... 4.5V to 11V

Junction Temperature Range .......... -40℃ to +150℃

Operating Temperature Range .......... -40℃ to +125℃

NOTES:

1. Ensure that $V_{SSA}$ and $V_{SSB}$ are connected to GND when the corresponding DAC group operates in the positive output voltage range.
2. Ensure that $V_{CCA}$ and $V_{CCB}$ are connected to GND when the corresponding DAC group operates in the negative output voltage range.

## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## OVERSTRESS CAUTION

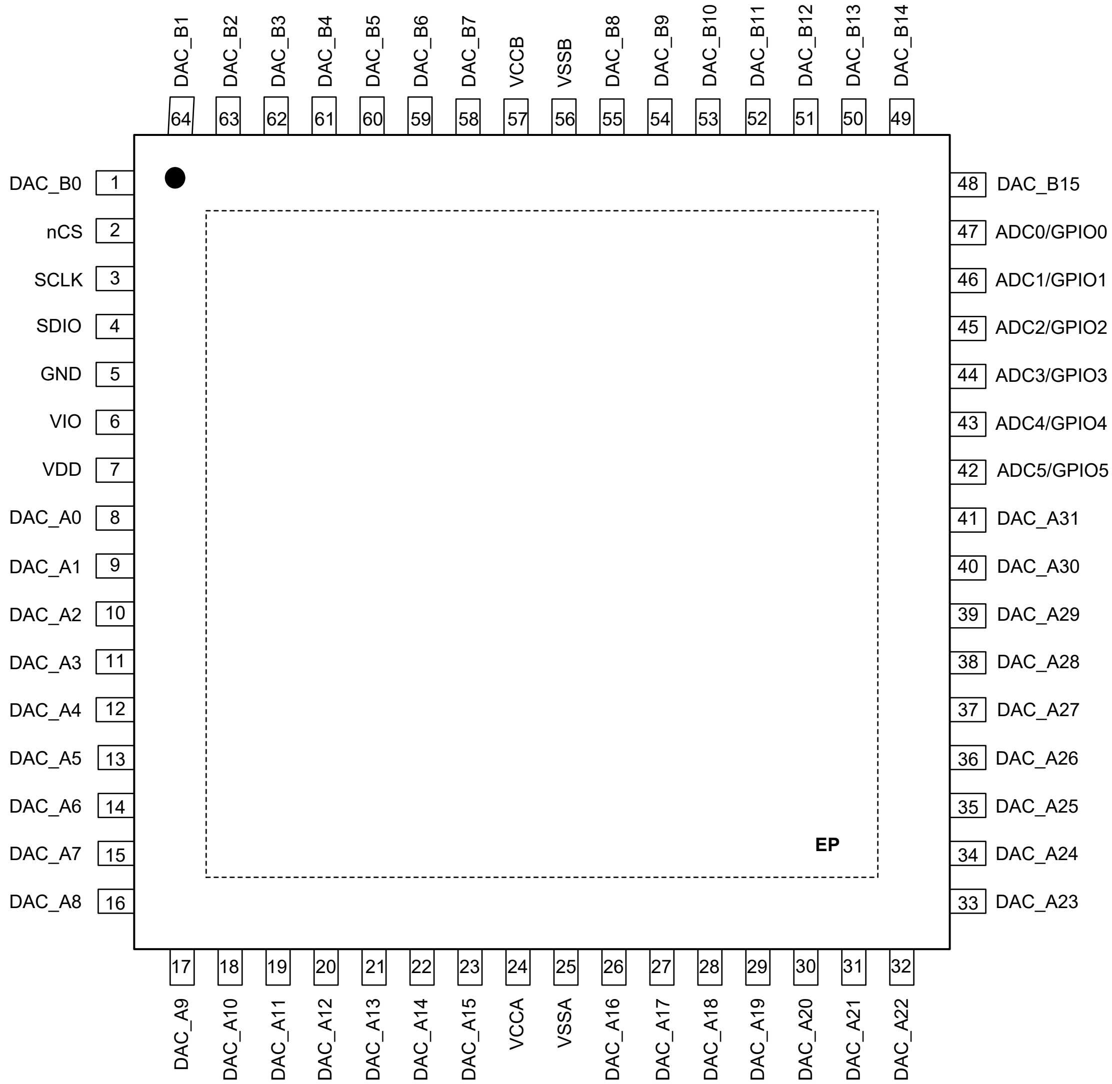
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TQFP-10×10-64L (Exposed Pad)

## PIN DESCRIPTION

| PIN | NAME | TYPE [1] | FUNCTION |
|---|---|---|---|
| 1 | DAC_B0 | O | DAC Output Group B. The output has the same range and clamp voltage. |
| 2 | nCS | I | Chip Select Signal. Active low. |
| 3 | SCLK | I | Serial Clock Input. |
| 4 | SDIO | I/O | Serial Data Input/Output. |
| 5 | GND | G | Ground. |
| 6 | VIO | P | Digital Input/Output Power Supply. It can be operated from 1.65V to 3.6V. |
| 7 | VDD | P | Analog Power Supply. It can be operated from 4.5V to 5.5V. |

## PIN DESCRIPTION (continued)

| PIN | NAME | TYPE (1) | FUNCTION |
|---|---|---|---|
| 8 | DAC_A0 | O | DAC Output Group A. The output has the same range and clamp voltage. |
| 9 | DAC_A1 | O | |
| 10 | DAC_A2 | O | |
| 11 | DAC_A3 | O | |
| 12 | DAC_A4 | O | |
| 13 | DAC_A5 | O | |
| 14 | DAC_A6 | O | |
| 15 | DAC_A7 | O | |
| 16 | DAC_A8 | O | |
| 17 | DAC_A9 | O | |
| 18 | DAC_A10 | O | |
| 19 | DAC_A11 | O | |
| 20 | DAC_A12 | O | |
| 21 | DAC_A13 | O | |
| 22 | DAC_A14 | O | |
| 23 | DAC_A15 | O | |
| 24 | VCCA | P | Positive Analog Supply. For the DAC group A output buffers, 0V to 11V. |
| 25 | VSSA | P | Negative Analog Supply. For the DAC group A output buffers, -11V to 0V. |
| 26 | DAC_A16 | O | DAC Output Group A. The output has the same range and clamp voltage. |
| 27 | DAC_A17 | O | |
| 28 | DAC_A18 | O | |
| 29 | DAC_A19 | O | |
| 30 | DAC_A20 | O | |
| 31 | DAC_A21 | O | |
| 32 | DAC_A22 | O | |
| 33 | DAC_A23 | O | |
| 34 | DAC_A24 | O | |
| 35 | DAC_A25 | O | |
| 36 | DAC_A26 | O | |
| 37 | DAC_A27 | O | |
| 38 | DAC_A28 | O | |
| 39 | DAC_A29 | O | |
| 40 | DAC_A30 | O | |
| 41 | DAC_A31 | O | |

## PIN DESCRIPTION (continued)

| PIN | NAME | TYPE [(1)] | FUNCTION |
|---|---|---|---|
| 42 | ADC5 /GPIO5 | I/O | Multi-Function Pin. ADC Input 5 (Default). Or the pin can be configured as a GPIO5.<br>GPIO5: When used as a GPIO, it can be configured as nALARMIN input pin. See GPIO configuration section. |
| 43 | ADC4 /GPIO4 | I/O | Multi-Function Pin. ADC Input 4 (Default). Or the pin can be configured as a GPIO4.<br>GPIO4: When used as a GPIO, it can be configured as nDAV output pin, active low for ADC data available indicator. See GPIO configuration section. |
| 44 | ADC3 /GPIO3 | I/O | Multi-Function Pin. ADC Input 3 (Default). Or the pin can be configured as a GPIO3.<br>GPIO3: When used as a GPIO, it can be configured as nADCTRIG input pin, active low for external ADC conversion trigger. See GPIO configuration section. |
| 45 | ADC2 /GPIO2 | I/O | Multi-Function Pin. ADC Input 2 (Default). Or the pin can be configured as a GPIO2.<br>GPIO2: When used as a GPIO, it can be configured as nALARMOUT output pin. And it's open-drain output and active low for global alarm output. See GPIO configuration section. |
| 46 | ADC1 /GPIO1 | I/O | Multi-Function Pin. ADC Input 1 (Default). Or the pin can be configured as a GPIO1.<br>GPIO1: When used as a GPIO, it can be configured as nCLEARB input pin, active low for DAC group B clear control signal. See GPIO configuration section. |
| 47 | ADC0 /GPIO0 | I/O | Multi-Function Pin. ADC Input 0 (Default). Or the pin can be configured as a GPIO0.<br>GPIO0: When used as a GPIO, it can be configured as nCLEARA input pin, active low for DAC group A clear control signal. See GPIO configuration section. |
| 48 | DAC_B15 | O | DAC Output Group B. The output has the same range and clamp voltage. |
| 49 | DAC_B14 | O | |
| 50 | DAC_B13 | O | |
| 51 | DAC_B12 | O | |
| 52 | DAC_B11 | O | |
| 53 | DAC_B10 | O | |
| 54 | DAC_B9 | O | |
| 55 | DAC_B8 | O | |
| 56 | VSSB | P | Negative Analog Supply. For the DAC group B output buffers, -11V to 0V. |
| 57 | VCCB | P | Positive Analog Supply. For the DAC group B output buffers, 0V to 11V. |
| 58 | DAC_B7 | O | DAC Output Group B. The output has the same range and clamp voltage. |
| 59 | DAC_B6 | O | |
| 60 | DAC_B5 | O | |
| 61 | DAC_B4 | O | |
| 62 | DAC_B3 | O | |
| 63 | DAC_B2 | O | |
| 64 | DAC_B1 | O | |
| Exposed Pad | EP | — | Exposed pad should be soldered to PCB board and connected to GND. |

NOTE:
1. I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 4.5V to 5.5V, $V_{IO}$ = 1.65V to 3.6V, positive output ranges: $V_{CC(A,B)}$ = 4.5V to 11V, $V_{SS(A,B)}$ = GND, negative output ranges: $V_{SS(A,B)}$ = -11V to -4.5V, $V_{CC(A,B)}$ = GND, and DAC outputs unloaded, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DAC DC Characteristics** [1] | | | | | | |
| Resolution | | | 12 | | | Bits |
| Full-Scale Output Voltage Range | | | -10 | | 0 | V |
| | | | -5 | | 0 | |
| | | | 0 | | 5 | |
| | | | 0 | | 10 | |
| Differential Nonlinearity | DNL | Specified 12-bit monotonic | -0.99 | | 1 | LSB |
| Integral Nonlinearity | INL | Positive output ranges | -6.3 | | 4.2 | LSB |
| | | Negative output ranges | -6 | | 6.9 | |
| **Positive Output Ranges** | | | | | | |
| Total Unadjusted Error [1] | TUE | | -1.8 | 0.14 | 1.2 | %FSR |
| Offset Error | | | -94 | 9 | 123 | mV |
| Offset Error Temperature Drift | | | | ±1.5 | | ppm/℃ |
| Gain Error | | | -2 | -0.26 | 1.5 | %FSR |
| Gain Error Temperature Drift | | | | ±5 | | ppm/℃ |
| Zero-Scale Error | | All zeros code | 0 | 12 | 87 | mV |
| Zero-Scale Error Temperature Drift | | | | ±1.2 | | ppm/℃ |
| Full-Scale Error | | All ones code | -2 | -0.15 | 1.8 | %FSR |
| Full-Scale Error Temperature Drift | | | | ±3 | | ppm/℃ |
| **Negative Output Ranges** | | | | | | |
| Total Unadjusted Error [1] | TUE | | -0.9 | 0.15 | 2.2 | %FSR |
| Offset Error | | | -59 | 5 | 69 | mV |
| Offset Error Temperature Drift | | | | ±1.2 | | ppm/℃ |
| Gain Error | | | -2.5 | -0.23 | 2.1 | %FSR |
| Gain Error Temperature Drift | | | | ±5 | | ppm/℃ |
| Zero-Scale Error | | All ones code | -56 | -18 | 0 | mV |
| Zero-Scale Error Temperature Drift | | | | ±5 | | ppm/℃ |
| Negative Full-Scale Error | | All zeros code | -2.2 | 0.3 | 2.6 | %FSR |
| Negative Full-Scale Error Temperature Drift | | | | 3.6 | | ppm/℃ |

NOTE:
1. This fits between codes 32 to 4064 (10V full-scale ranges) and 64 to 4032 (5V full-scale ranges).

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 4.5V to 5.5V, $V_{IO}$ = 1.65V to 3.6V, positive output ranges: $V_{CC(A,B)}$ = 4.5V to 11V, $V_{SS(A,B)}$ = GND, negative output ranges: $V_{SS(A,B)}$ = -11V to -4.5V, $V_{CC(A,B)}$ = GND, and DAC outputs unloaded, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DAC Output Buffer Characteristics** | | | | | | |
| Load Current (2) | | Source with 1V headroom from $V_{CC(A,B)}$, normal-current mode | 8.5 | | | mA |
| | | Sink with 1V headroom from $V_{SS(A,B)}$, normal-current mode | 13 | | | |
| Short-Circuit Current (2) | | Low-current mode | | ±11 | | mA |
| | | Normal-current mode (default) | | ±45 | | |
| Capacitive Load Stability (3) | | | 0 | | 10 | nF |
| DC Output Impedance | | Midscale code | | 1 | | Ω |
| Output Voltage Settling Time | | $R_L$ = 2kΩ, $C_L$ = 200pF, positive output ranges: 0V to 2.5V step to within 2.5mV, negative output ranges: -5V to -2.5V step to within 2.5mV | | 7 | | μs |
| | | $R_L$ = 2kΩ, $C_L$ = 200pF, 1/4 to 3/4 scale settling to ±0.5LSB | | 11 | | |
| Slew Rate | SR | 1/4 to 3/4 scale transition, 10% to 90% | | 0.5 | | V/μs |
| Output Noise | | 0.1Hz to 10Hz, midscale code | | 60 | | $\mu V_{PP}$ |
| Output Noise Density | | 1kHz, midscale code | | 450 | | $nV/\sqrt{Hz}$ |
| AC PSRR | | Midscale code, f = 60Hz, amplitude = $200mV_{PP}$ superimposed on $V_{DD}$ | | 59 | | dB |
| | | Midscale code, f = 60Hz, amplitude = $200mV_{PP}$ superimposed on $V_{CC(A,B)}$ | | 89 | | |
| | | Midscale code, f = 60Hz, amplitude = $200mV_{PP}$ superimposed on $V_{SS(A,B)}$ | | 86 | | |
| DC PSRR | | Midscale code, ±10% variation on all supplies | | 1 | | mV/V |
| Power-On Overshoot | | $V_{SS(A,B)}$ = GND, $V_{CC(A,B)}$ = 0V to 11V, 2ms ramp | | 80 | | mV |
| | | $V_{CC(A,B)}$ = GND, $V_{SS(A,B)}$ = 0V to -11V, 2ms ramp | | 100 | | |
| Channel-to-Channel DC Crosstalk | | Measured DAC output at midscale, all other DAC outputs at full-scale | | 0.5 | | mV |
| **Clamp Output Characteristics** | | | | | | |
| Load Current | | DAC output buffers in power-down mode, sink with 2V headroom from $V_{SS(A,B)}$ | 13 | | | mA |
| **Auto-Range Threshold Detector** | | | | | | |
| $V_{SS}$ Threshold Detector | $V_{SSTH}$ | $V_{SS}$ supply failure detection | -4.2 | | -3 | V |
| $V_{CC}$ Threshold Detector | $V_{CCTH}$ | $V_{CC}$ supply failure detection | 2.5 | | 3.5 | V |

NOTES:

2. Overload condition protection. The junction temperature can be exceeded during current limit. Operating beyond the specified maximum junction temperature may damage the reliability of the chip.
3. Guaranteed by design. Not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 4.5V to 5.5V, $V_{IO}$ = 1.65V to 3.6V, positive output ranges: $V_{CC(A,B)}$ = 4.5V to 11V, $V_{SS(A,B)}$ = GND, negative output ranges: $V_{SS(A,B)}$ = -11V to -4.5V, $V_{CC(A,B)}$ = GND, and DAC outputs unloaded, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ADC Characteristics** | | | | | | |
| Resolution | | | 12 | | | Bits |
| Full-Scale Input Voltage Range | | | 0 | | 5 | V |
| | | | 0 | | 2.5 | |
| Differential Nonlinearity | DNL | Specified 12-bit monotonic | -0.99 | ±0.5 | 1 | LSB |
| Integral Nonlinearity | INL | | -2 | ±0.5 | 2 | LSB |
| Offset Error | | After calibration | -13 | -3.8 | 5 | LSB |
| Offset Error Match | | | | ±1 | | LSB |
| Gain Error | | | -0.47 | ±0.05 | 0.56 | %FSR |
| Gain Error Match | | | | ±1 | | LSB |
| Input Capacitance | | | | 15 | | pF |
| Input Bias Current | | ADC not converting | -10 | | 10 | μA |
| Conversion Time | | | 1.875 | | | μs |
| Acquisition Time | | | 2.125 | | | μs |
| Conversion Rate | | | | | 250 | kSPS |
| Throughput Rate | | SCLK = 20MHz | | | 250 | kSPS |
| **Temperature Sensor Characteristics** | | | | | | |
| Operating Junction Temperature | | | -40 | | 150 | ℃ |
| Accuracy | | $T_J$ = -40℃ to +125℃ | -3.5 | ±1.5 | 3.5 | ℃ |
| Resolution | | LSB size | | 0.0625 | | ℃ |
| Update Time | | 32 conversions per second | | 31.25 | | ms |
| **ADCn/GPIOn Digital Characteristics** | | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{IO}$ = 1.65V | 0.8 × $V_{IO}$ | | | V |
| | | $V_{IO}$ = 3.6V | 0.8 × $V_{IO}$ | | | |
| Input Low Voltage | $V_{IL}$ | $V_{IO}$ = 1.65V | | | 0.2 × $V_{IO}$ | V |
| | | $V_{IO}$ = 3.6V | | | 0.2 × $V_{IO}$ | |
| **Serial Interface Characteristics** | | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{IO}$ = 1.65V | 0.8 × $V_{IO}$ | | | V |
| | | $V_{IO}$ = 3.6V | 0.8 × $V_{IO}$ | | | |
| Input Low Voltage | $V_{IL}$ | $V_{IO}$ = 1.65V | | | 0.2 × $V_{IO}$ | V |
| | | $V_{IO}$ = 3.6V | | | 0.2 × $V_{IO}$ | |
| Input Current | | | | 2 | | μA |
| Input Pin Capacitance | | | | 6 | | pF |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 0.2mA | $V_{IO}$ - 0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 0.2mA | | | 0.4 | V |
| Output Pin Capacitance | | | | 6 | | pF |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 4.5V to 5.5V, $V_{IO}$ = 1.65V to 3.6V, positive output ranges: $V_{CC(A,B)}$ = 4.5V to 11V, $V_{SS(A,B)}$ = GND, negative output ranges: $V_{SS(A,B)}$ = -11V to -4.5V, $V_{CC(A,B)}$ = GND, and DAC outputs unloaded, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Requirements** | | | | | | |
| $V_{DD}$ Supply Current | $I_{VDD}$ | No DAC load, all DACs in positive range at midscale code, ADC at the fastest auto conversion rate, temperature sensor enabled and static SPI | | | 14 | mA |
| $V_{CCA}$ Supply Current per Group | $I_{VCCA}$ | | | | 12 | mA |
| $V_{CCB}$ Supply Current per Group | $I_{VCCB}$ | | | | 6 | mA |
| $V_{SS}$ Supply Current per Group | $I_{VSS}$ | | | | 0 | mA |
| $V_{IO}$ Supply Current | $I_{VIO}$ | | | | 7 | μA |
| Power Consumption | | | | | 300 | mW |
| $V_{DD}$ Supply Current | $I_{VDD}$ | No DAC load, all DACs in negative range at midscale code, ADC at the fastest auto conversion rate, temperature sensor enabled and static SPI | | | 15 | mA |
| $V_{CC}$ Supply Current per Group | $I_{VCC}$ | | | | 0 | mA |
| $V_{SSA}$ Supply Current per Group | $I_{VSSA}$ | | -14 | | | mA |
| $V_{SSB}$ Supply Current per Group | $I_{VSSB}$ | | -7 | | | mA |
| $V_{IO}$ Supply Current | $I_{VIO}$ | | | | 7 | μA |
| Power Consumption | | | | | 320 | mW |
| $V_{DD}$ Supply Current | $I_{VDD}$ | Power-down, mixed DAC range mode | | | 5 | mA |
| $V_{CCA}$ Supply Current per Group | $I_{VCCA}$ | | | | 0.5 | mA |
| $V_{CCB}$ Supply Current per Group | $I_{VCCB}$ | | | | 0.25 | mA |
| $V_{SSA}$ Supply Current per Group | $I_{VSSA}$ | | -3 | | | mA |
| $V_{SSB}$ Supply Current per Group | $I_{VSSB}$ | | -2 | | | mA |
| $V_{IO}$ Supply Current | $I_{VIO}$ | | | | 7 | μA |
| Power Consumption | | | | | 100 | mW |

# TIMING REQUIREMENTS

($V_{DD}$ = 4.5V to 5.5V, $V_{IO}$ = 1.65V to 3.6V, positive output ranges: $V_{CC(A,B)}$ = 4.5V to 11V, $V_{SS(A,B)}$ = GND, negative output ranges: $V_{SS(A,B)}$ = -11V to -4.5V, $V_{CC(A,B)}$ = GND, and DAC outputs unloaded, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| SCLK Frequency | $f_{SCLK}$ | 3V ≤ $V_{IO}$ < 3.6V | | | | 20 | MHz |
| | | 1.7V ≤ $V_{IO}$ < 3V | | | | 10.5 | |
| nCS High Time | $t_1$ | | | 25 | | | ns |
| nCS Setup Time | $t_2$ | | | 25 | | | ns |
| nCS Hold Time | $t_3$ | | | 25 | | | ns |
| SDO Driven to Tri-State | $t_4$ | | | 0 | | 55 | ns |
| SCLK Low Time | $t_5$ | | | 23 | | | ns |
| SCLK High Time | $t_6$ | | | 23 | | | ns |
| SDI Setup Time | $t_7$ | | | 7 | | | ns |
| SDI Hold Time | $t_8$ | | | 7 | | | ns |
| SDO Tri-State to Driven | $t_9$ | SDOZDD = 0 | $V_{IO}$ = 1.65V to 1.9V | | | 55 | ns |
| | | | $V_{IO}$ = 1.9V to 3.6V | | | 45 | |
| | | SDOZDD = 1 | $V_{IO}$ = 1.65V to 1.9V | | | 58 | |
| | | | $V_{IO}$ = 1.9V to 3.6V | | | 48 | |
| SDO Output Delay | $t_{10}$ | | | | | 45 | ns |

# TIMING DIAGRAM

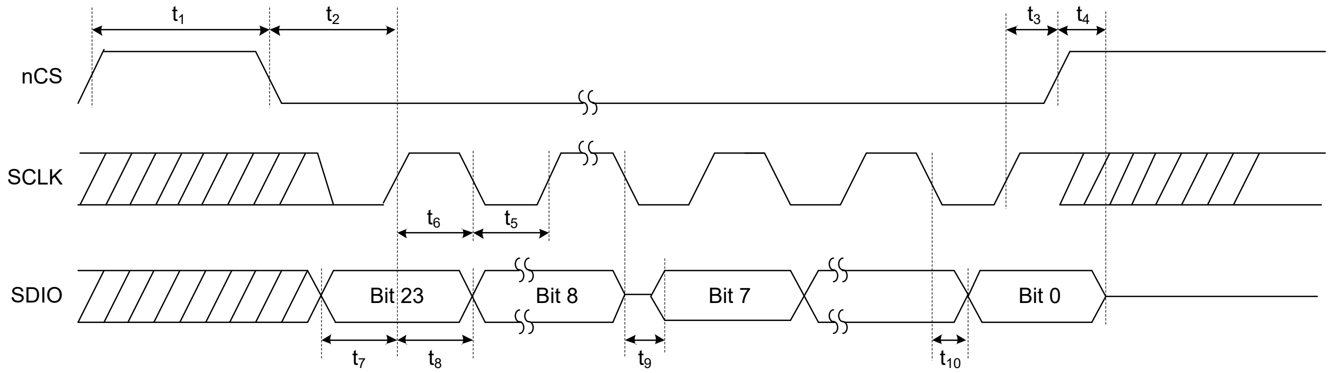



**Figure 1. Three-Wire Serial Interface Read/Write Timing Diagram**

## SWITCHING CHARACTERISTICS

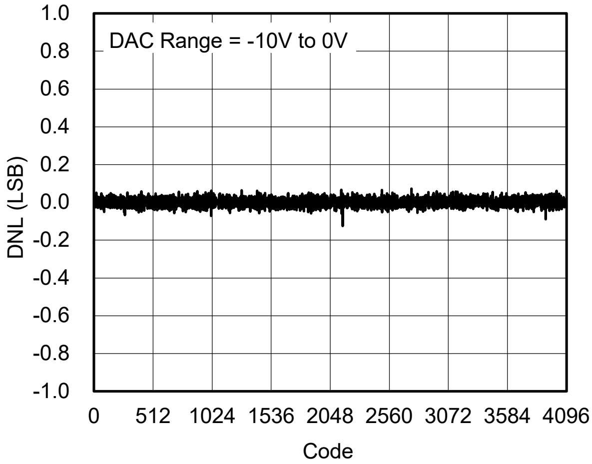
($V_{DD}$ = 4.5V to 5.5V, $V_{IO}$ = 1.65V to 3.6V, positive output ranges: $V_{CC(A,B)}$ = 4.5V to 11V, $V_{SS(A,B)}$ = GND, negative output ranges: $V_{SS(A,B)}$ = -11V to -4.5V, $V_{CC(A,B)}$ = GND, and DAC outputs unloaded, $T_J$ = -40℃ to +125℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RESET Characteristics** | | | | | | |
| Device Ready Wait Time | $t_{AMCRDY}$ | Time for valid serial interface access, measured from reset event | | 100 | 250 | µs |
| **ALARM Characteristics** | | | | | | |
| nALARMOUT Response Time | $t_{ALMOUT}$ | Measured from nALARMIN trigger, 4.7kΩ pull-up to $V_{IO}$ | | 65 | 70 | ns |
| **DAC Characteristics** | | | | | | |
| DAC Clear Response Time | $t_{DACCLR}$ | Measured from nALARMIN trigger (1), DAC outputs unloaded | | 1.5 | 2.5 | µs |
| | | Measured from nCLEAR(A,B) trigger (1), DAC outputs unloaded | | 1.5 | 2.5 | |
| **ADC Characteristics** | | | | | | |
| ADC Wait Time | $t_{ADCWAIT}$ | Time from when the ADC enters IDLE state to when the ADC is ready for trigger | 2 | | | µs |
| nADCTRIG Pulse Width | $t_{ADCTRIG}$ | | 20 | | | ns |

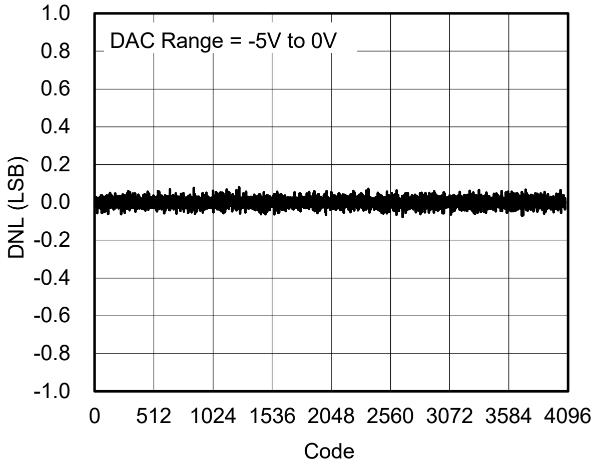
NOTE:
1. To keep nCLEAR(A,B) and nALARMIN function valid for DAC outputs, the signal nCLEAR(A,B) and nALARMIN should be kept LOW once trigger occur.

# TYPICAL PERFORMANCE CHARACTERISTICS

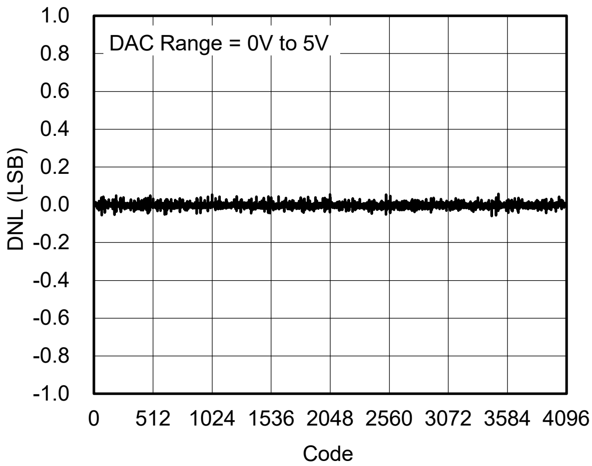
DAC DNL vs. Digital Input Code



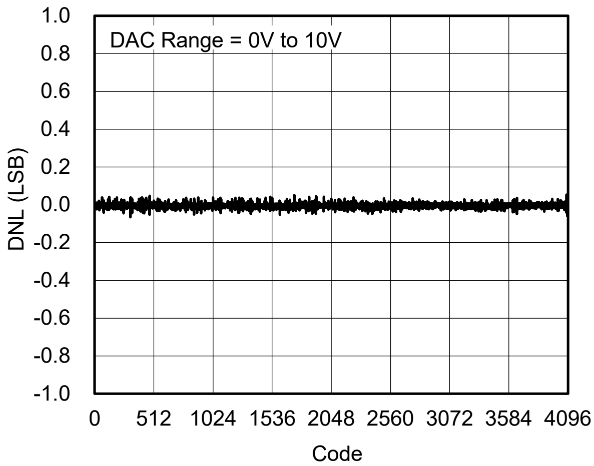

DAC DNL vs. Digital Input Code



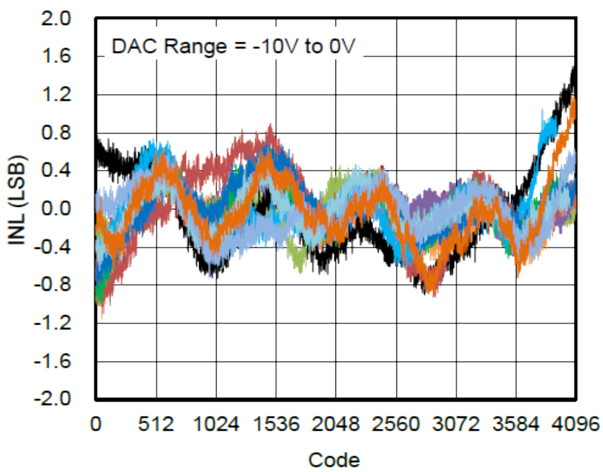

DAC DNL vs. Digital Input Code



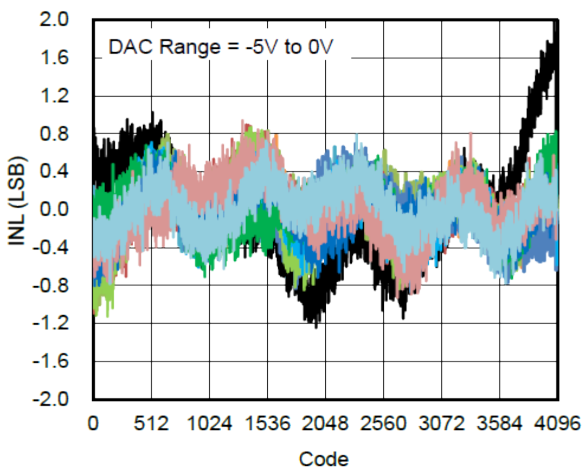

DAC DNL vs. Digital Input Code




DAC INL vs. Digital Input Code

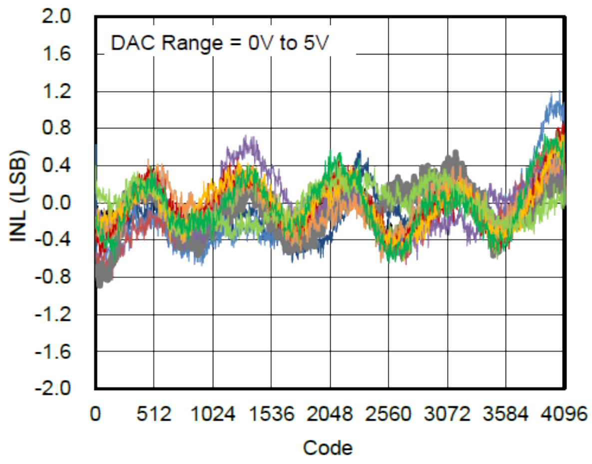



DAC INL vs. Digital Input Code

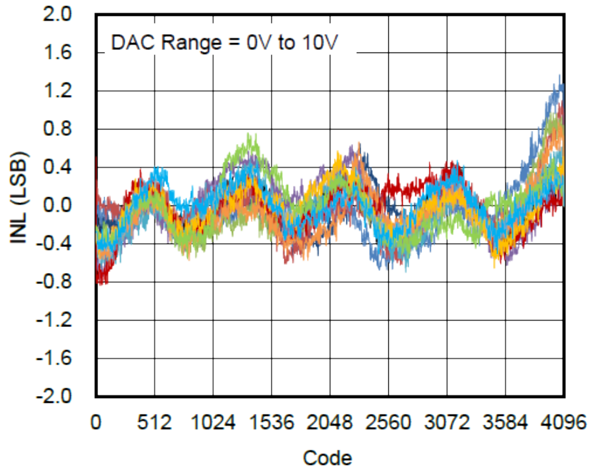


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

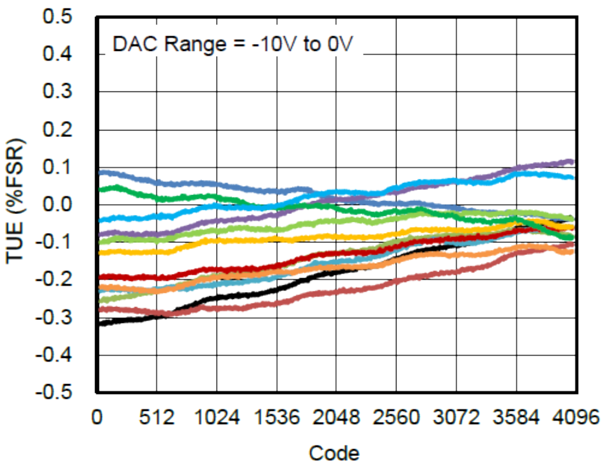
DAC INL vs. Digital Input Code



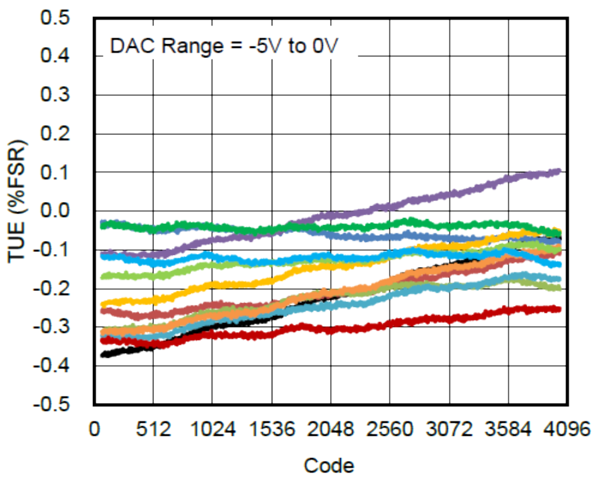

DAC INL vs. Digital Input Code



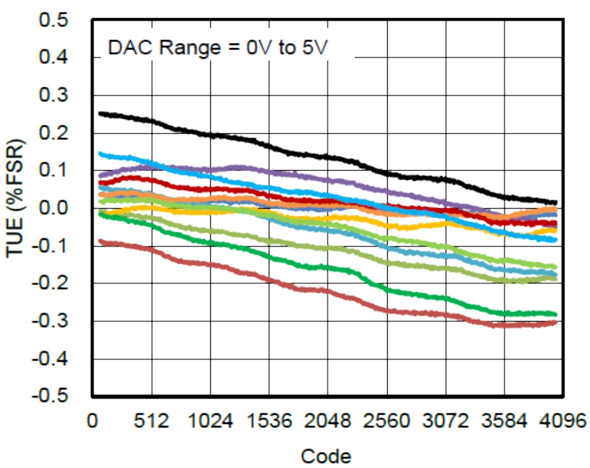

DAC TUE vs. Digital Input Code



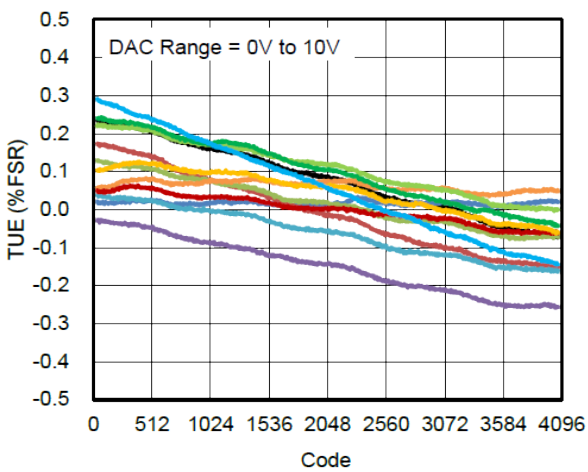

DAC TUE vs. Digital Input Code



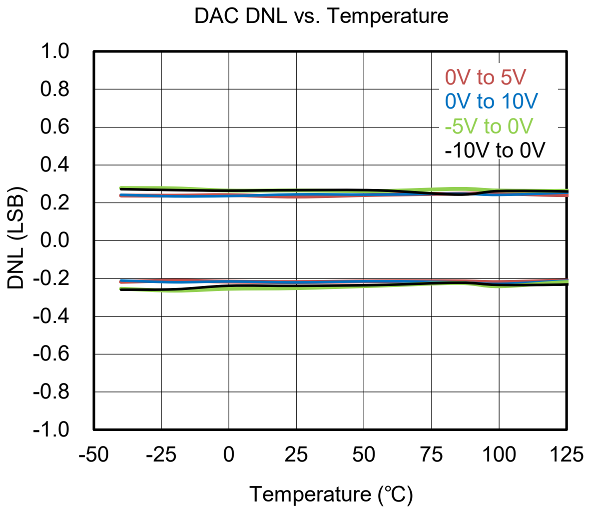

DAC TUE vs. Digital Input Code

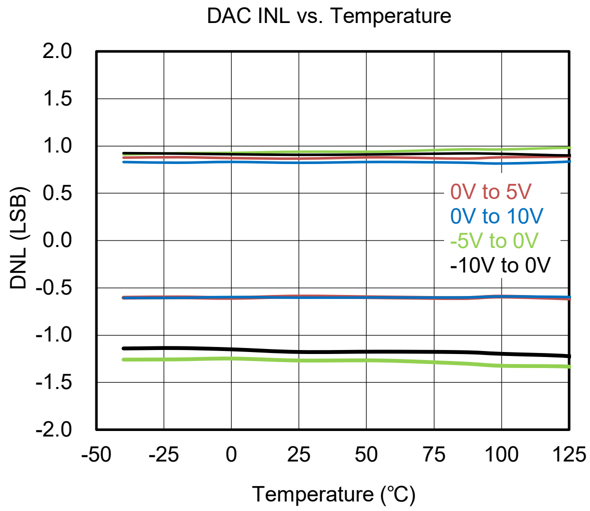


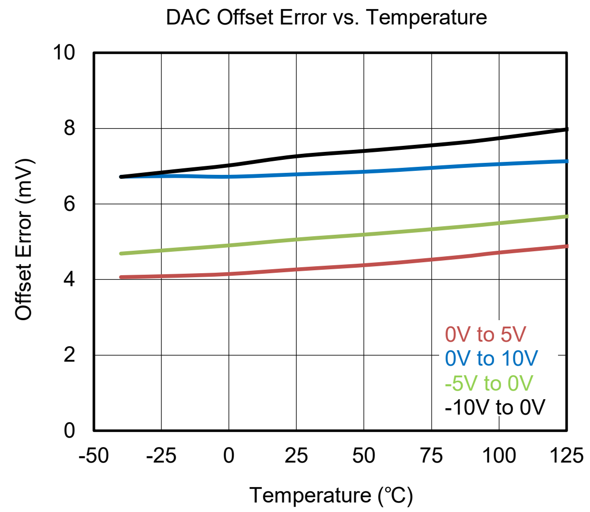

DAC TUE vs. Digital Input Code

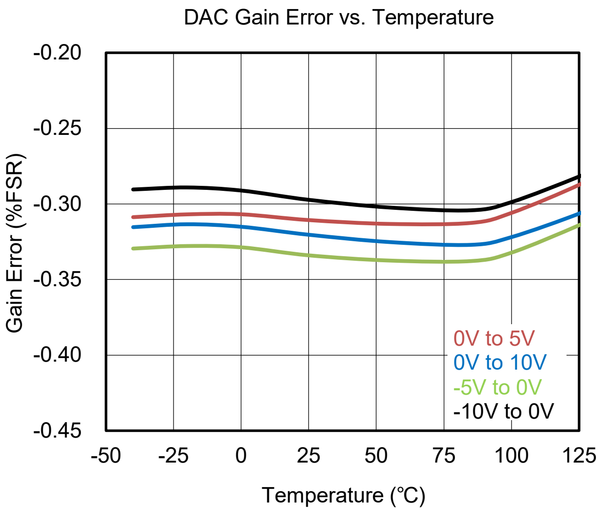


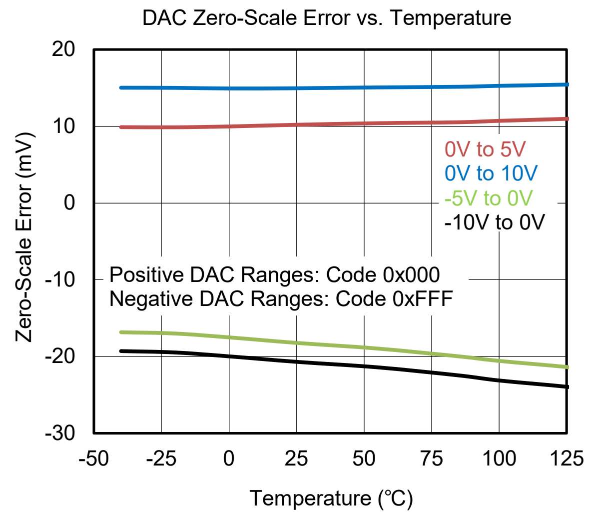
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

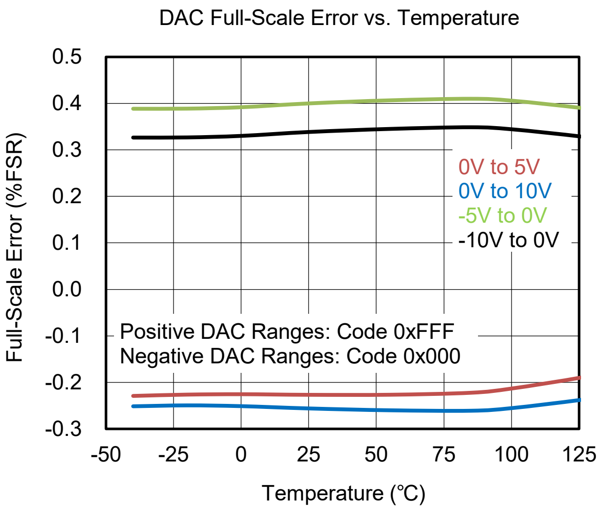


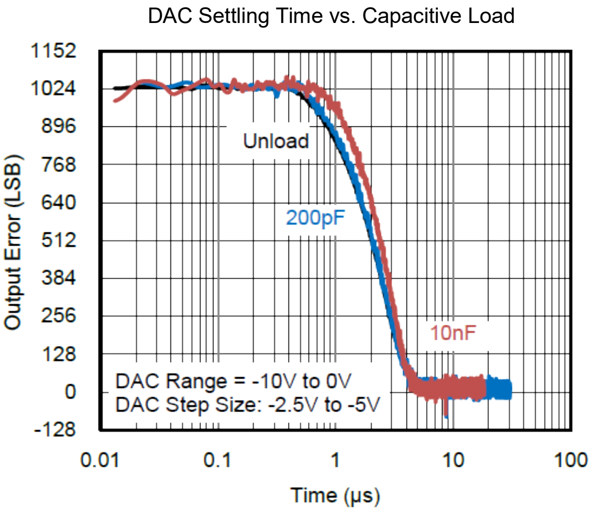



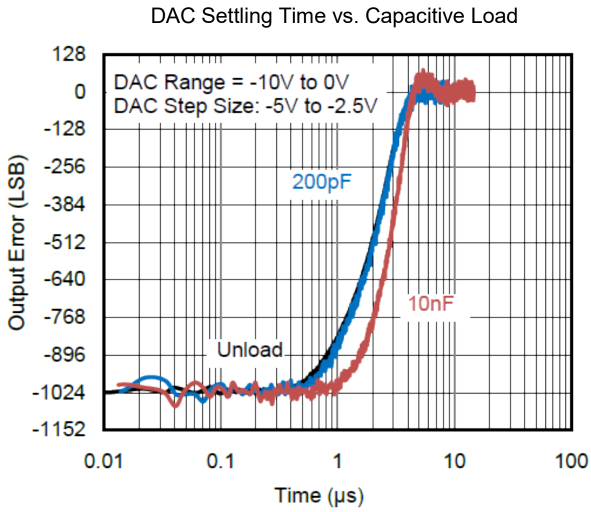



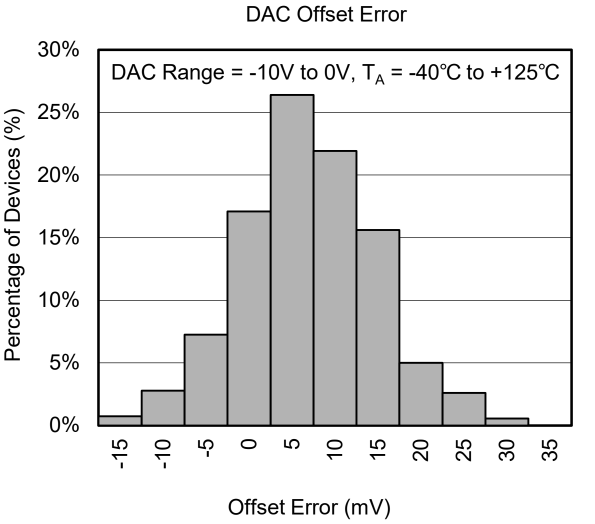



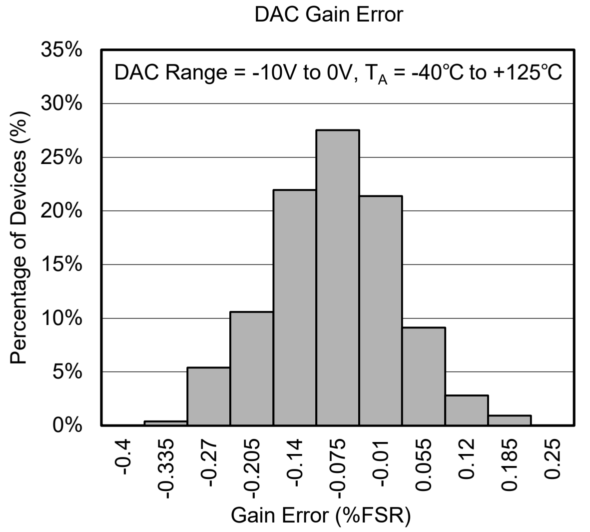



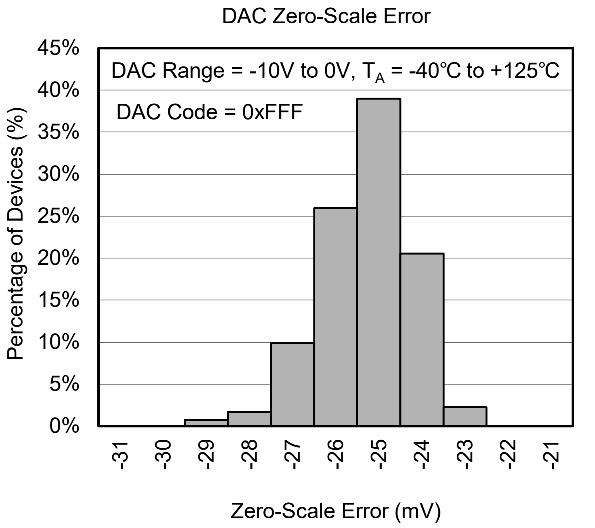
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

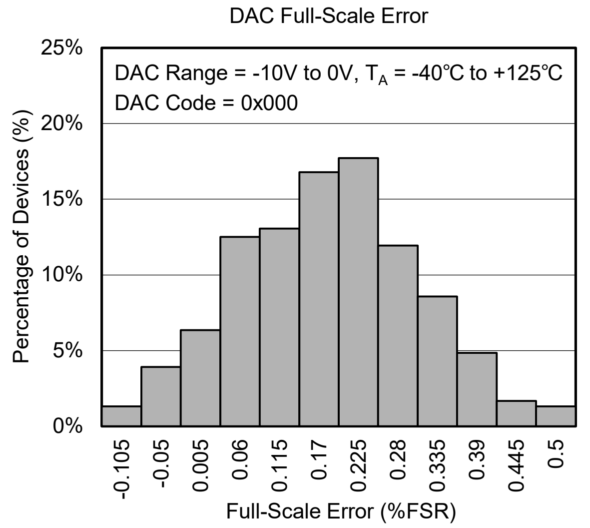


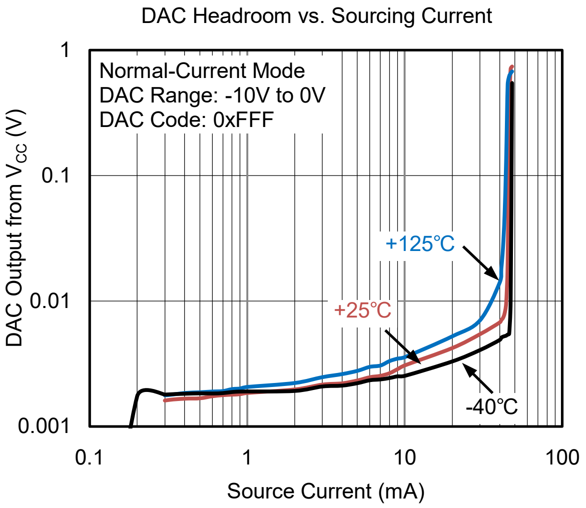



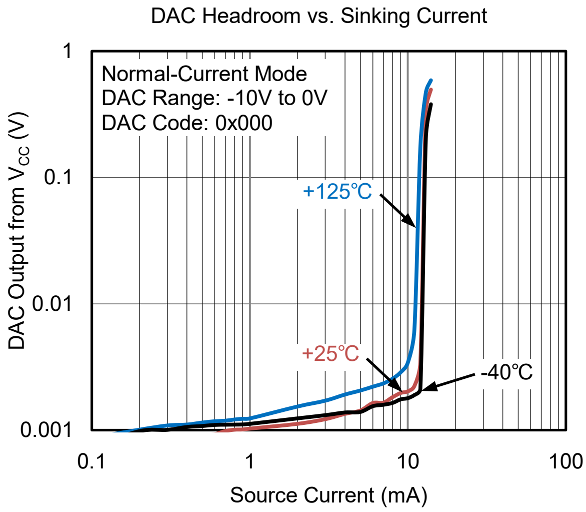



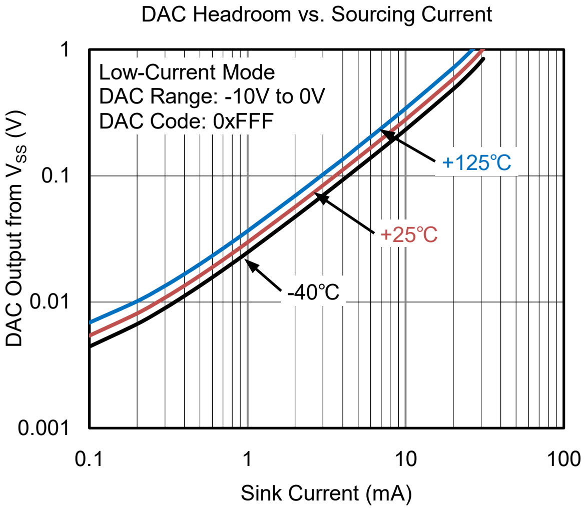



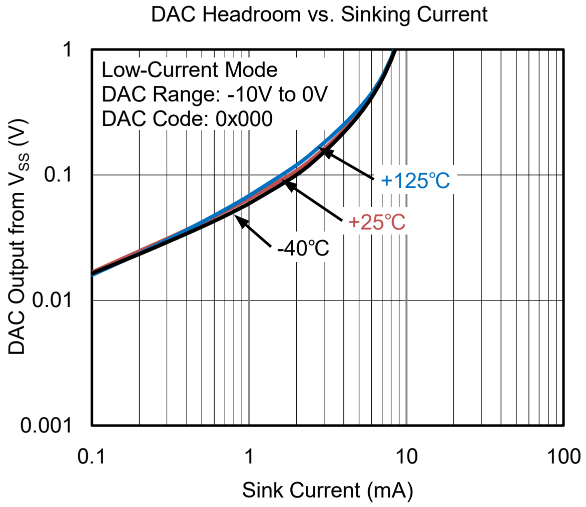



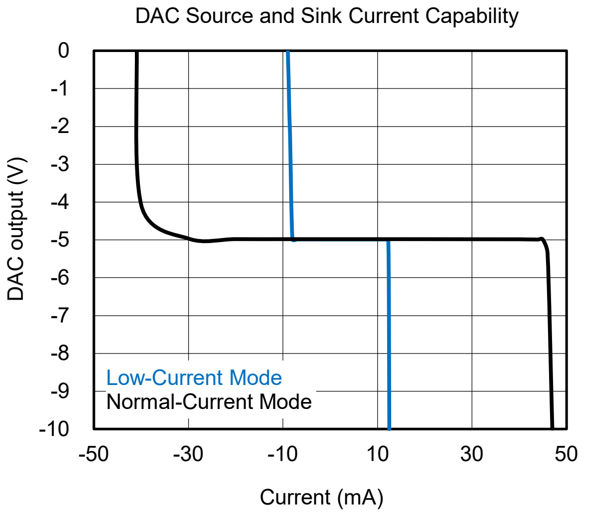
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

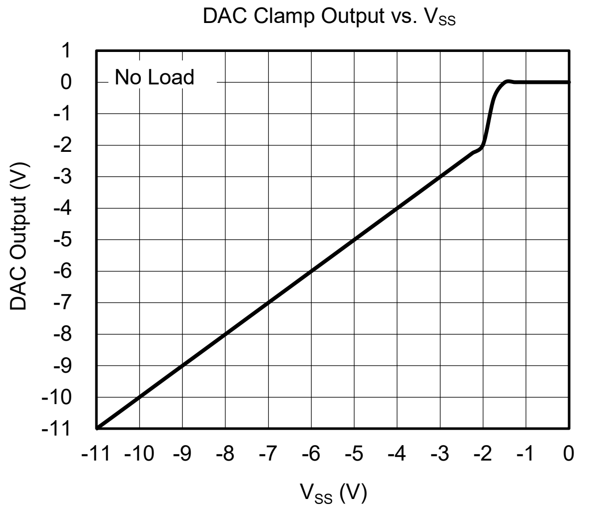


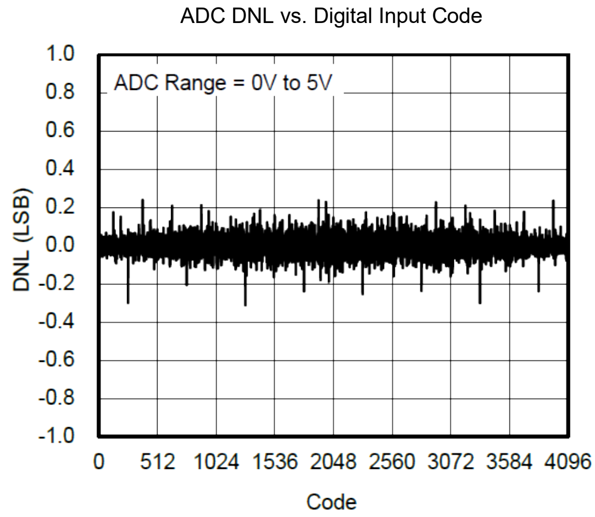



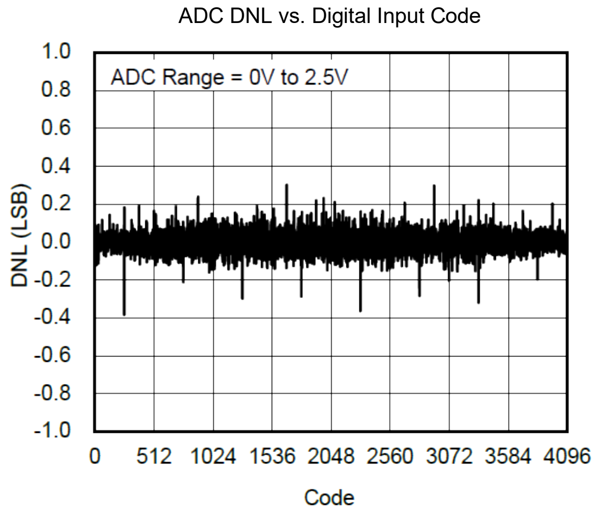



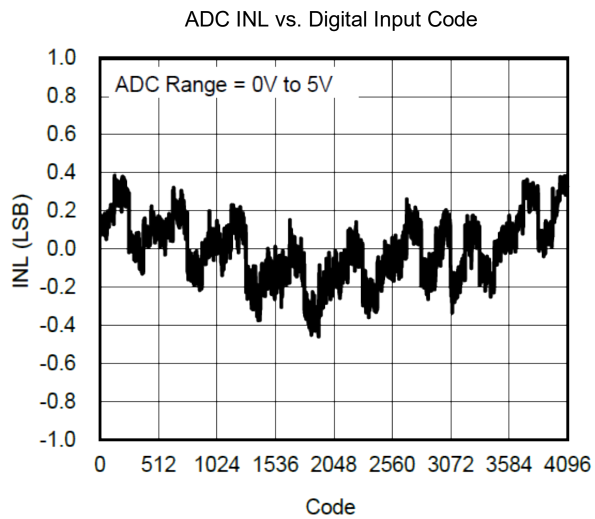



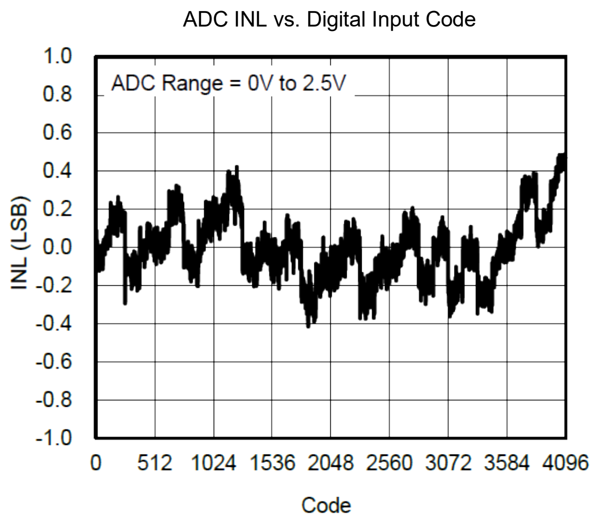



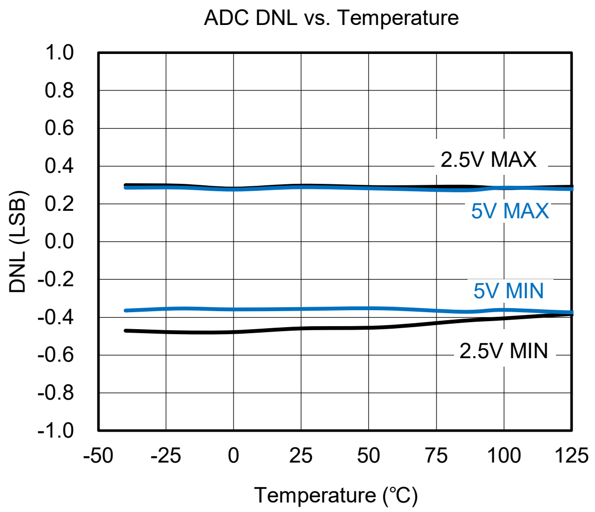
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

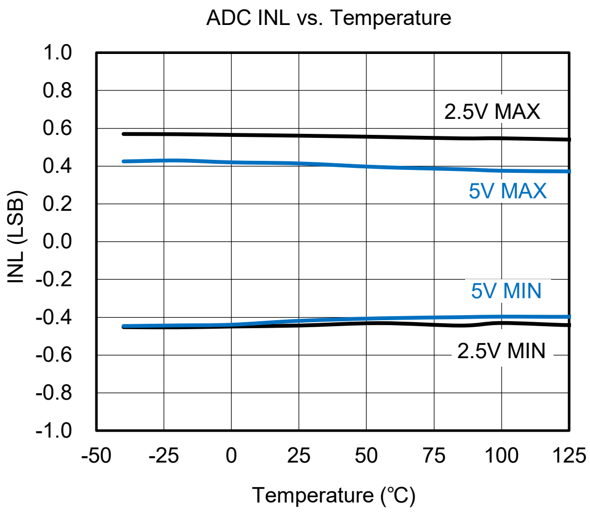


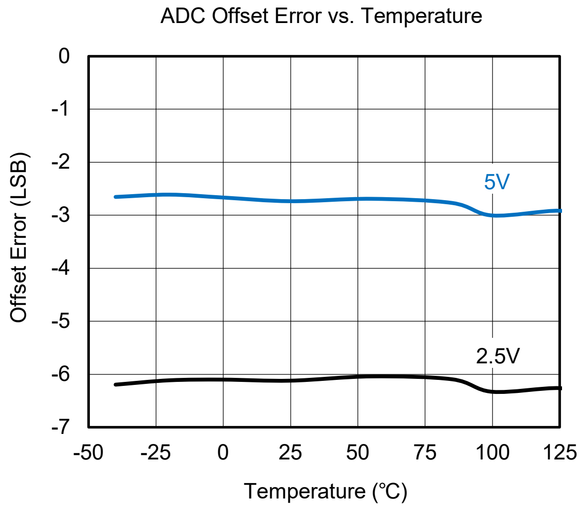



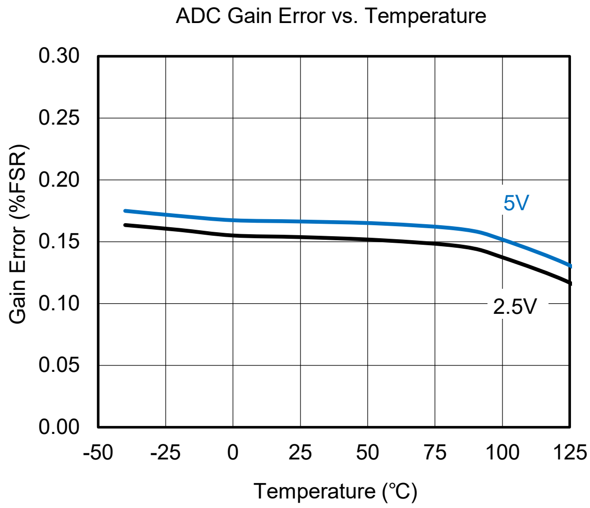



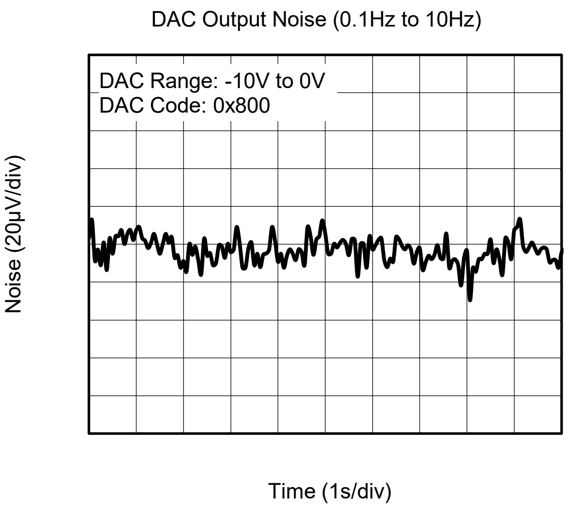



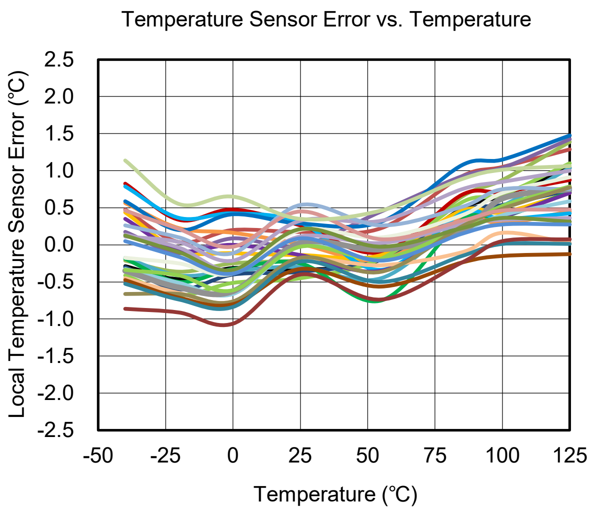



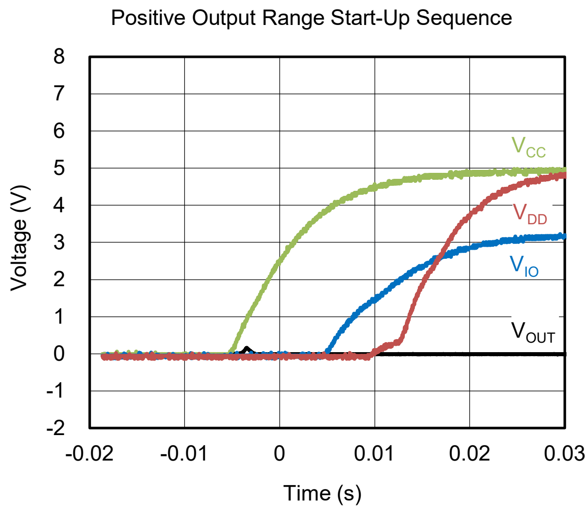
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

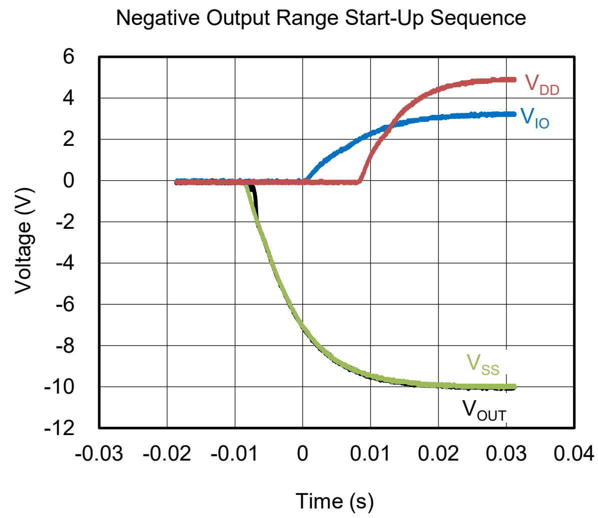


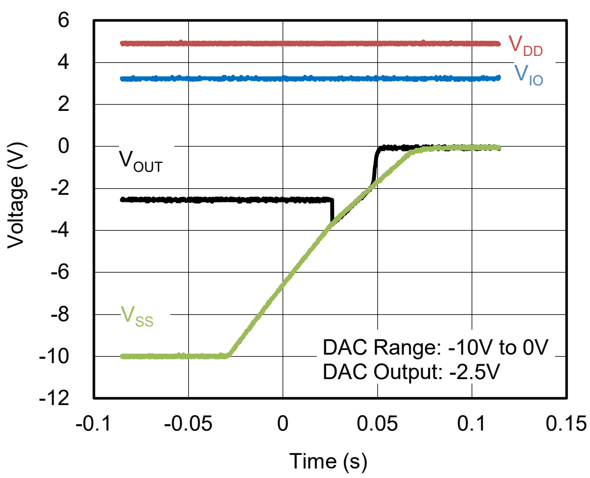



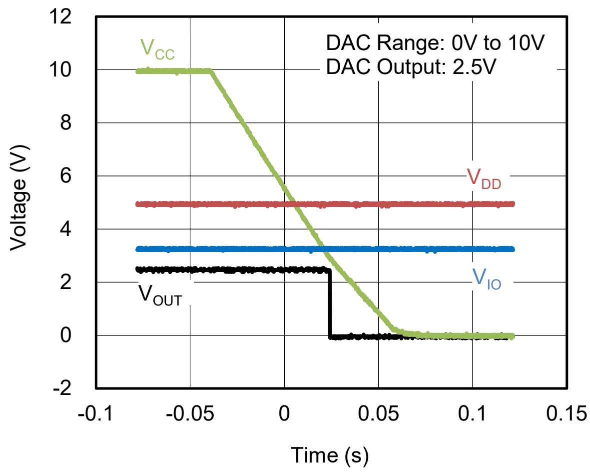



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

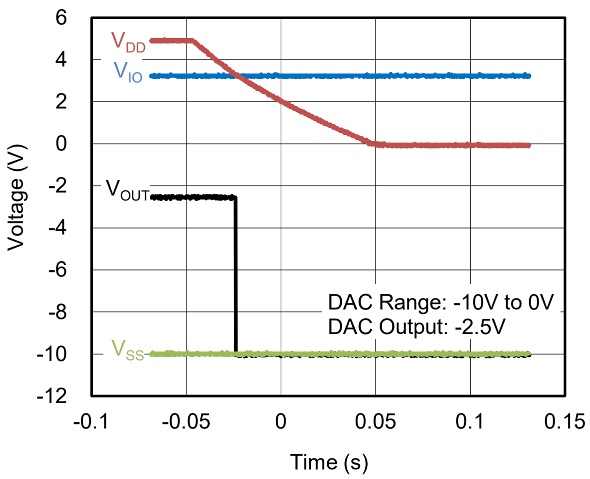
$V_{SS}$ Supply Collapse Response



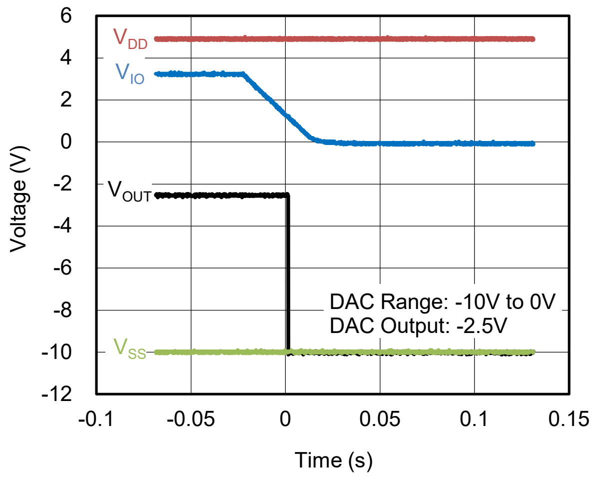

$V_{CC}$ Supply Collapse Response



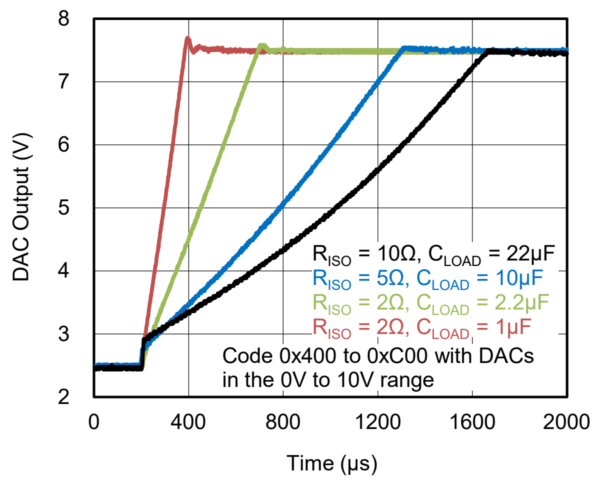

$V_{DD}$ Supply Collapse Response



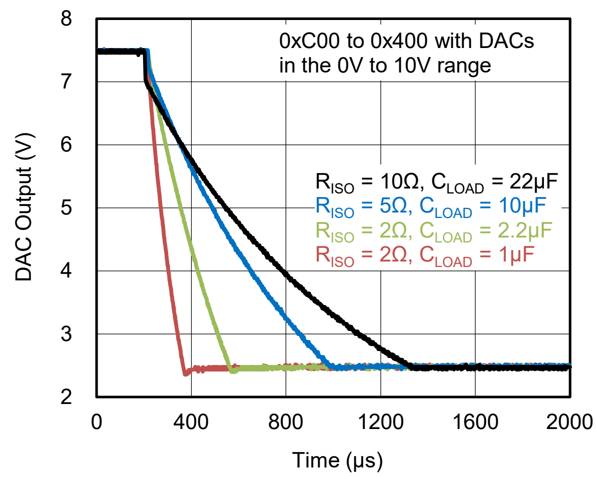

$V_{IO}$ Supply Collapse Response




DAC Settling Time vs. Load Capacitance




DAC Settling Time vs. Load Capacitance



# FUNCTIONAL BLOCK DIAGRAM

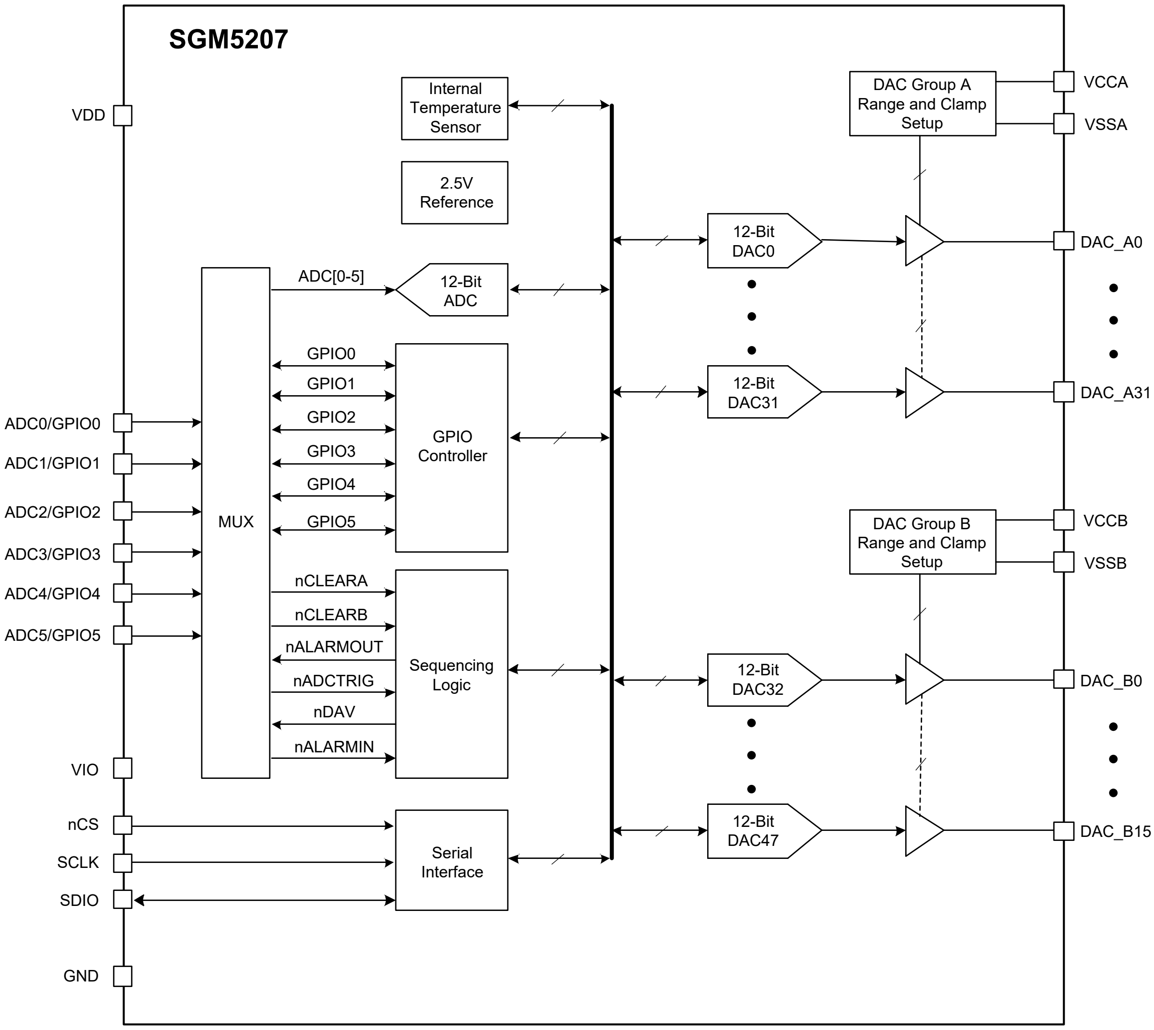



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Digital-to-Analog Converters (DACs)

The SGM5207 has 48 channels DAC outputs. These DACs are divided into two groups. Each channel DAC simplified equal circuit is shown in Figure 3. The core DAC is powered by VDD. The output buffer is powered by VCCA and VSSA (or VCCB and VSSB).

Under different configuration, the DAC output ideal range is shown in Table 1. The data format is straight binary.

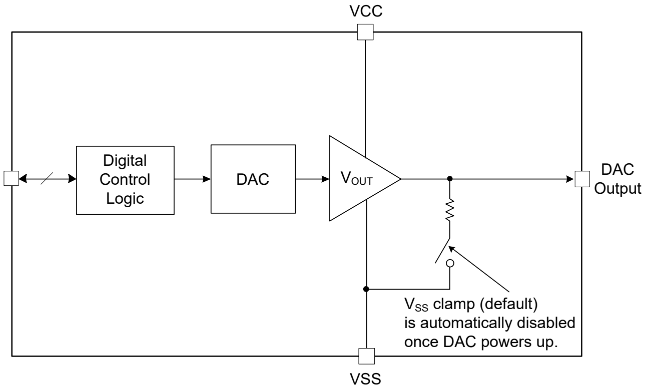



**Figure 3. DAC Block Diagram**

***Auto-Range Detection***

In a power-up event, the output range of each DAC group is automatically set by the auto-range detector.

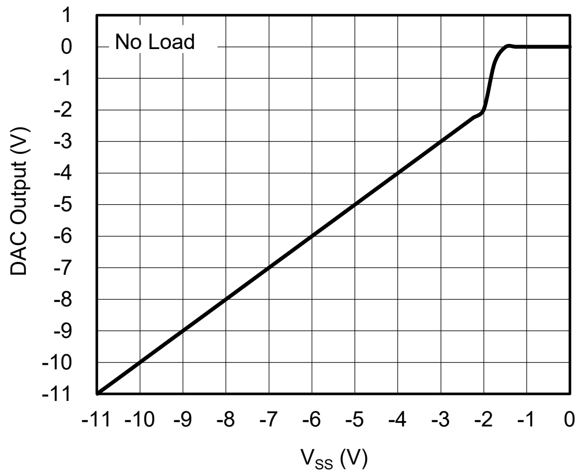



**Figure 4. DAC Clamp Output vs. $V_{SS}$**

***Power Supply Monitoring***

The available voltage range of DAC is shown in Table 2. During operation, power monitoring circuit continuously monitors the power supply voltage, if $V_{CC(A,B)}$ or $V_{SS(A,B)}$ is below the specified threshold associated with the supply configuration, $V_{DD}$ < 4.5V or $V_{IO}$ < 1.65V, a reset event is produced, and all DAC outputs return to the $V_{SS}$ clamp mode.

**Table 1. DAC Data Format**

| DAC Data Register | | DAC Output Voltage (V) | | | |
|---|---|---|---|---|---|
| Binary | Hex | 0V to 5V Range ($V_{CC}$ = 5.5V, $V_{SS}$ = GND) | 0V to 10V Range ($V_{CC}$ = 11V, $V_{SS}$ = GND) | -5V to 0V Range ($V_{SS}$ = -5.5V, $V_{CC}$ = GND) | -10V to 0V Range ($V_{SS}$ = -11V, $V_{CC}$ = GND) |
| 0000 0000 0000 | 0x000 | 0 | 0 | -5 | -10 |
| 0000 0000 0001 | 0x001 | 0.00122 | 0.00244 | -4.99878 | -9.99756 |
| 1000 0000 0000 | 0x800 | 2.5 | 5 | -2.5 | -5 |
| 1111 1111 1110 | 0xFFE | 4.99756 | 9.99512 | -0.00244 | -0.00488 |
| 1111 1111 1111 | 0xFFF | 4.99878 | 9.99756 | -0.00122 | -0.00244 |

**Table 2. Valid Supply Matrix**

| DAC Group Supply Configuration | Supply | |
|---|---|---|
| | $V_{CC(A,B)}$ | $V_{SS(A,B)}$ |
| Invalid Configuration | 0V ≤ $V_{CC}$ < 4.5V | -4.5V < $V_{SS}$ ≤ 0V |
| $V_{CC}$ Configuration | 4.5V ≤ $V_{CC}$ ≤ 11V | $V_{SS}$ = 0V |
| Invalid Configuration | 4.5V ≤ $V_{CC}$ ≤ 11V | $V_{SS}$ < 0V |
| $V_{SS}$ Configuration | $V_{CC}$ = 0V | -11V ≤ $V_{SS}$ < -4.5V |
| Invalid Configuration | $V_{CC}$ > 0V | -11V ≤ $V_{SS}$ < -4.5V |

## DETAILED DESCRIPTION (continued)

**DAC Clear Operation**

Each DAC can go to a clear status that can be triggered by hardware and software. Once a DAC is in clear state, it outputs a zero-code voltage that is accordance with the configured operating range. When it is in clear state, DAC buffer and active register will hold the data before going to clear event, but these registers reading out is returned with zero-code.

When the chip is in clear state, the DAC buffer and active register can be updated by writing. Once the DAC exits the clear status, the DAC output is updated with setting.

The DAC clear event can be trigged by nCLEARA and nCLEARB pin or an alarm event. These trigger conditions must be configured in DAC clear enable registers.

Once the alarm bit is cleared and there is no other alarm events are triggered, the DAC exits clear status and update output with DAC active register.

### Analog-to-Digital Converter (ADC)

The SGM5207 has a 12-bit SAR ADC, which can be configured with six inputs through a multiplexer. The ADC is drove by internal oscillator.

**ADCn/GPIOn Multiplexer**

The SGM5207 has six ADCn/GPIOn flexible inputs, which can be configured as ADC input, GPIO, and logic control pin. After reset, these pins default are ADC inputs.

**ADC Transfer Function**

Please see Table 3 for details.

**ADC Offset Calibration**

The SGM5207 has an offset calibration function. When the chip is reset, the calibration is performed automatically if the ADC is the first triggered. It takes about 3μs to complete a calibration.

After the first ADC trigger and calibration, if it needs to be calibrated again, the ADC_CAL bit needs to be set in the ADC configuration register before issuing an ADC trigger.

**ADC Sequencing**

The SGM5207 ADC has two conversion modes, direct mode and auto mode. After reset, the default mode is direct mode. In both modes, the ADC channels are selected by ADC MUX configuration register.

In direct mode, an ADC trigger signal (software or hardware) is issued, all selected channels are converted in sequence, and then ADC goes to IDLE state. The ADC waits in IDLE state until a new trigger signal is issued.

In auto mode, the conversion cycle is triggered by an ADC trigger signal (software or hardware). All selected channels will be converted in sequence. When a cycle is completed, a new cycle will be started automatically. It won't stop until a second trigger signal occurs.

In both working modes, the ADC associated registers which include ADC configuration register, false alarm configuration register, ADC MUX configuration register, ADC high and low limit registers, and ADC hysteresis registers must be updated in ADC IDLE state. After any register is updated, the host controller must wait at least 2μs before sending a new ADC trigger signal.

**Table 3. Transfer Characteristics**

| Input Voltage | Code | Description | Ideal Output Code |
|---|---|---|---|
| ≤ 1LSB | NFSC | Negative Full-Scale Code | 0x000 |
| 1LSB to 2LSBs | NFSC + 1 | — | 0x001 |
| $(V_{RANGE}/2)$ to $(V_{RANGE}/2)$ + 1LSB | MC | Midcode | 0x800 |
| $(V_{RANGE}/2)$ + 1LSB to $(V_{RANGE}/2)$ + 2LSBs | MC + 1 | — | 0x801 |
| ≥ $V_{RANGE}$ - 1LSB | PFSC | Positive Full-Scale Code | 0xFFF |

## DETAILED DESCRIPTION (continued)

### ADC Synchronization

The ADC trigger signal can be software (ADC_TRIG bit in the ADC trigger register) or hardware (nADCTRIG, pin 44). To use nADCTRIG, it must be configured accordingly in the GPIO configuration register. Once the pin is configured, a trigger signal is active on the falling edge of nADCTRIG pin.

In auto mode, to update the ADC data registers, there is no need for synchronization between the SGM5207 and the host controller. Only issue an ADC_UPDATE command (in the register update register) and all ADC data registers are updated with the latest available data. The ADC_UPDATE bit will reset automatically. To read all ADC data out, the register reading sequence needs to be followed.

In direct mode, the ADC data registers should be read out during the ADC is in IDLE state. The ADC provides an indicator signal to report ADC status. The indicator signal can be hardware (nDAV pin which must be configured in GPIO configuration register) or software (DAVF bit in the general status register). Please refer to Figure 5 for details

After a direct mode conversion is complete and ADC returns to the IDLE state, nDAV pin is set to low and DAVF bit is set to 1 immediately. The pin and flag will reset automatically if a new conversion starts or one of ADC data registers is read.

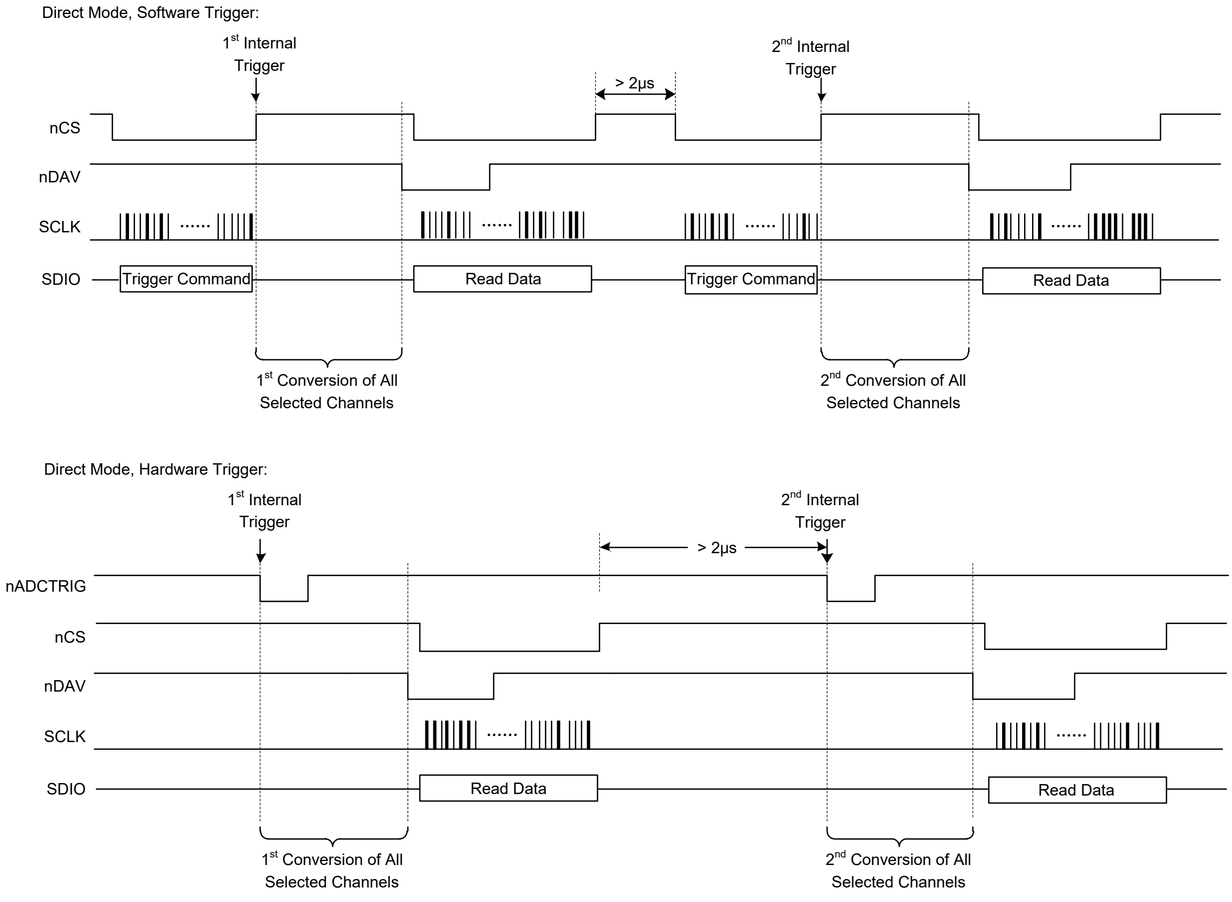



**Figure 5. ADC Direct Mode Trigger Synchronization**

# DETAILED DESCRIPTION (continued)

## Internal Temperature Sensor

The SGM5207 has an on-chip temperature sensor. It's a separate 12-bit ADC. The available report temperature range is -64℃ to 191.9375℃. The data resolution is 0.0625℃. The accuracy range only from -40℃ to +125℃. The output data has two sections (represented by two bytes), the integral number and the fractional number.

The high byte is the integral section, which is 1℃ resolution. The data format is a bias straight binary. See details in Table 4.

The low byte is the fractional section, which is 0.0625℃ resolution. The data format is a straight binary. See details in Table 5.

To update the temperature data registers, there is no need for synchronization between the SGM5207 and the host controller. Only issuing a LT_UPDATE command (in the register update register), all temperature data registers are updated with the latest available data. The LT_UPDATE bit will reset automatically. To read all temperature data out, need follow registers reading sequence.

**Table 4. LT_DATA[11:4] Data Format**

| Temperature (℃) | Internal Temperature Data Register LT_DATA[11:4] Value (1) | |
|---|---|---|
| | Binary | Hex |
| -64 | 0000 0000b | 00h |
| -50 | 0000 1110b | 0Eh |
| -25 | 0010 0111b | 27h |
| -1 | 0011 1111b | 3Fh |
| 0 | 0100 0000b | 40h |
| 1 | 0100 0001b | 41h |
| 10 | 0100 1010b | 4Ah |
| 25 | 0101 1001b | 59h |
| 50 | 0111 0010b | 72h |
| 75 | 1000 1011b | 8Bh |
| 100 | 1010 0100b | A4h |
| 125 | 1011 1101b | BDh |
| 127 | 1011 1111b | BFh |
| 150 | 1101 0110b | D6h |
| 175 | 1110 1111b | EFh |
| 191 | 1111 1111b | FFh |

NOTE: 1. 1℃ resolution.

**Table 5. LT_DATA[3:0] Data Format**

| Temperature (℃) | Internal Temperature Data Register LT_DATA[3:0] Value (1) | |
|---|---|---|
| | Binary | Hex |
| 0 | 0000b | 0h |
| 0.0625 | 0001b | 1h |
| 0.1250 | 0010b | 2h |
| 0.1875 | 0011b | 3h |
| 0.2500 | 0100b | 4h |
| 0.3125 | 0101b | 5h |
| 0.3750 | 0110b | 6h |
| 0.4375 | 0111b | 7h |
| 0.5000 | 1000b | 8h |
| 0.5625 | 1001b | 9h |
| 0.6250 | 1010b | Ah |
| 0.6875 | 1011b | Bh |
| 0.7500 | 1100b | Ch |
| 0.8125 | 1101b | Dh |
| 0.8750 | 1110b | Eh |
| 0.9375 | 1111b | Fh |

NOTE: 1. 0.0625℃ resolution. All available values are shown.

### Example for Extended Binary-to-Decimal Temperature Data Calculation

For LT_DATA[11:4] conversion, take 0110 0011 as an example: The binary value is converted into the hexadecimal value. And then remove the offset value 64 (℃).

The specific calculation process is shown as follows:

$0110\ 0011b \rightarrow 63h \rightarrow (6 \times 16^1) + (3 \times 16^0) = 99$

$99 - 64 = 35$

For LT_DATA[3:0] conversion, take 0101 as an example: The binary value is converted into the decimal value.

The specific calculation process is shown as follows:

$0101b \rightarrow (0 \times 1/2)^1 + (1 \times 1/2)^2 + (0 \times 1/2)^3 + (1 \times 1/2)^4$

$= 0.3125$

### Example for Extended Decimal-to-Binary Temperature Data Calculation

Add 64℃ from the required temperature to adjust for the extended binary format.

Example 1 (84℃): 84℃ - (- 64℃) = 148℃

Example 2 (-10℃): -10℃ - (- 64℃) = 54℃

For positive temperature adjusted results
(Example 1: 84℃ →148℃):

148℃/(1℃/count) = 148 → 94h → 1001 0100

For negative temperature adjusted results
(Example 2: -10℃ → 54℃):

54℃/(1℃/count) = 54 → 36h →0011 0110

# DETAILED DESCRIPTION (continued)

### Temperature Sensor Conversion Rate

The temperature conversion rate is list in Table 6. The conversion rate setting is the time interval between two conversions. It's not the temperature conversion time.

**Table 6. Temperature Sensor Conversion Rate (Address: 0x2F)**

| Value | Conversions per Second | Time (Seconds) |
|---|---|---|
| 00h | 0.0625 | 16 |
| 01h | 0.125 | 8 |
| 02h | 0.25 | 4 |
| 03h | 0.5 | 2 |
| 04h | 1 | 1 |
| 05h | 2 | 0.5 |
| 06h | 4 | 0.25 |
| 07h | 8 | 0.125 |
| 08h | 16 (default) | 0.0625 (default) |
| 09h | 32 | 0.03125 |

## Programmable Out-of-Range Alarms

The SGM5207 can continuously monitor kinds of inputs and give out alarms. The alarm sources include the ADC high and low limit, the temperature high and low limit, reference voltage and an external input signal (nALARMIN Alarm).

If any limit is exceeded (configured in according limit registers), set the corresponding alarm bit (in the alarm status registers). At the same time, the global alarm GALR bit (in the general status register) is set. A simple schematic is shown in Figure 6.

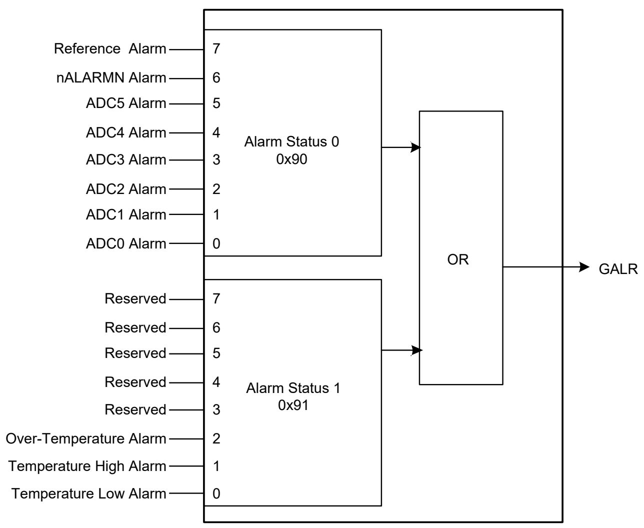



**Figure 6. Alarm Status Registers**

Except the nALARMIN bit, all the others can be latched by enabling the ALARM_LATCH_DIS bit (in the ALARMOUT source 1 register). Once the ALARM_LATCH_DIS bit is enabled, the alarm bits can be cleared by software reading the alarm status registers. If the exceeding alarm limit condition is still there, the alarm bit will be set again.

When the ALARM_LATCH_DIS is not enabled, the alarm bits are not latched, once the exceeding alarm limit condition is removed, the alarm bits will be cleared automatically.

All the alarms sources can be used to drive the nALARMOUT pin. nALARMOUT pin function is configured in the GPIO configuration register. Any alarm event used to activate the nALARMOUT pin must be enabled in the ALARMOUT source register. If an alarm source is enabled in the ALARMOUT source register, an out-of-limit is occurred, the status register according bit still is set.

All of the alarms can be used to trigger the enabled DACs to the clear state. To enable this function, DAC clear alarm source (in the DAC clear source register) and DACs to be cleared (set in the DAC clear enable registers) must be set accordingly. When a DAC clear alarm is triggered, selected DACs are set to be cleared. Once the alarm condition is removed, DACs outputs return to the previous status which it doesn't need any additional operations.

### Temperature Sensor Alarm Function

The temperature alarm status bits are shown in Table 7.

**Table 7. Temperature Alarm Status**

| Bits | Description |
|---|---|
| THERM_ALR | Over-Temperature Thermal Alarm |
| LTHIGH_ALR | Temperature High Limit Alarm |
| LTLOW_ALR | Temperature Low Limit Alarm |

The internal temperature high limit register (LT_HL[7:0]) sets the high limitation. The internal temperature low limit register (LT_LL[7:0]) sets the low limitation. The temperature sensor false alarm settings (LT_FALR[2:0] bits in the false alarm configuration register) set the violations times of alarm before an alarm event is set.

## DETAILED DESCRIPTION (continued)

The SGM5207 has an internal over-temperature thermal alarm, which is set in the thermal alarm high limit register (THERM_HL[7:0]). A hysteresis window can be set by the thermal alarm hysteresis register. It's shown in Figure 7.

### ADC Alarm Function

Each of ADC channels has independent input alarm monitoring units. The high and low limits are set in ADC high limit and low limit registers.

To prevent false alarm triggering, the consecutive violation alarm time is set in the false alarm configuration register.

A hysteresis window can be set by the ADC alarm hysteresis register. It's shown in Figure 8. The available range of hysteresis window is 0LSB to 127LSB.

### Internal Reference Alarm Function

The SGM5207 has an internal reference monitoring alarm, when the reference voltage is < 2.2V, an alarm (REF_ALR bit) is set in the alarm status 0 register. Before enabling ADC and DAC output, make sure to check the reference is working well.

### nALARMIN Alarm Function

The SGM5207 supports external alarm signal input, which needs configure nALARMIN pin in the GPIO configuration register. Once it's configured as nALARMIN input, this pin input is active low.

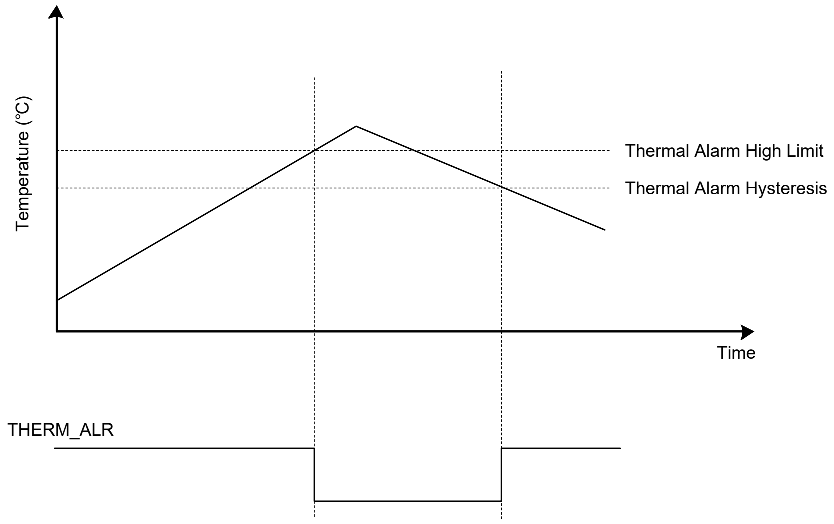



**Figure 7. Over-Temperature Alarm Hysteresis**

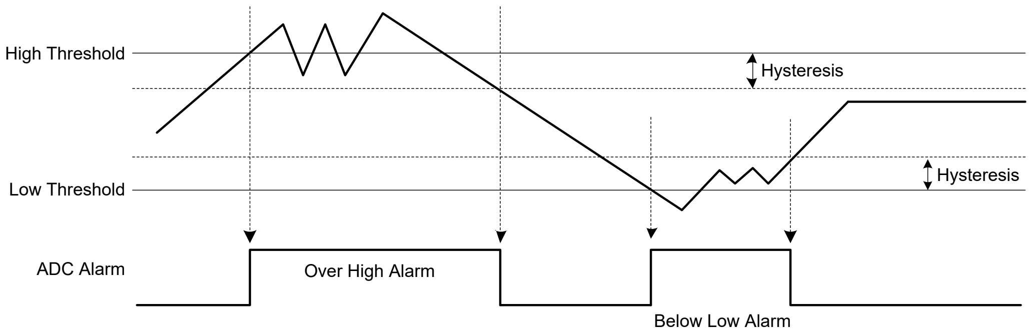



**Figure 8. ADC Alarm Hysteresis**

# DETAILED DESCRIPTION (continued)

## Flexible Input/Output (ADCn/GPIOn) Pins

The SGM5207 has six ADCn/GPIOn pins. Table 8 shows the functionality selection.

**Table 8. ADCn/GPIOn Pin Functionality**

| Configuration Bit | | ADCn/GPIOn Pin Function |
|---|---|---|
| GPIO | ADC MUX | |
| 0 | 0 | GPIO |
| 1 | 0 | Alternative Sequencing Signal |
| x | 1 | ADC Input |

When the ADCn/GPIOn pins are used as GPIO pins, these pins can alternatively be sequencing function pin. The alternative function of these pins is shown in Table 9.

**Table 9. ADCn/GPIOn Pin Alternative Functionality**

| Pin | Default Pin Name | Alternative Pin Name | Alternative Functionality |
|---|---|---|---|
| 42 | ADC5/GPIO5 | nALARMIN | Alarm Input |
| 43 | ADC4/GPIO4 | nDAV | ADC Data Available Indicator |
| 44 | ADC3/GPIO3 | nADCTRIG | External ADC Conversion Trigger |
| 45 | ADC2/GPIO2 | nALARMOUT | Global Alarm Output |
| 46 | ADC1/GPIO1 | nCLEARB | DAC Group B Clear Control Signal |
| 47 | ADC0/GPIO0 | nCLEARA | DAC Group A Clear Control Signal |

The ADCn/GPIOn pins are reset to default high-impedance.

## Device Functional Modes

The SGM5207 has two groups of DACs output. Each group can be configured separately. The chip can working in three modes: all-positive DAC range mode, all-negative DAC range mode and mixed DAC range mode.

### All-Positive DAC Range Mode

In the all-positive DAC range mode, each group DACs output must be in the range from VSSA (VSSB) to VCCA (VCCB). All available ranges are listed in Table 10. In this mode, two groups of DAC are not required working in the same power range.

**Table 10. Typical Configuration in All-Positive DAC Range Mode**

| Pin | Typical Connection | Notes |
|---|---|---|
| VDD | 4.5V to 5.5V | |
| VIO | 1.65V to 3.6V | $V_{IO} \le V_{DD}$ |
| VCCA | $4.5V \le V_{CCA} \le 11V$ | $V_{DACA} \le V_{CCA}$ |
| VCCB | $4.5V \le V_{CCB} \le 11V$ | $V_{DACB} \le V_{CCB}$ |
| VSSA | GND | |
| VSSB | GND | |
| Exposed Pad | GND | |

In the all-positive DAC range mode, when system is power-on reset, the auto-range detector will set all the DAC groups to default 0V to 5V range, whether the real power supply is 5V range or the real power is 10V range. After power-up, the 10V output range needs to be configured by software.

### All-Negative DAC Range Mode

In the all-negative DAC range mode, each group DACs output must be in the range from VSSA (VSSB) to VCCA (VCCB). All available ranges are listed in Table 11. In this mode, two groups of DAC are not required working in the same power range.

**Table 11. Typical Configuration in All-Negative DAC Range Mode**

| Pin | Typical Connection | Notes |
|---|---|---|
| VDD | 4.5V to 5.5V | |
| VIO | 1.65V to 3.6V | $V_{IO} \le V_{DD}$ |
| VCCA | GND | |
| VCCB | GND | |
| VSSA | $-11V \le V_{SSA} \le -4.5V$ | $V_{DACA} \ge V_{SSA}$ |
| VSSB | $-11V \le V_{SSB} \le -4.5V$ | $V_{DACB} \ge V_{SSB}$ |
| Exposed Pad | GND | |

In the all-negative DAC range mode, when system is power-on reset, the auto-range detector will set all the DAC groups to default -10V to 0V range, whether the real power supply is -10V range or the real power is -5V range. After power-up, the -5V output range needs to be configured by the software.

# DETAILED DESCRIPTION (continued)

### Mixed DAC Range Mode

In the mixed DAC range mode, each group DACs output must be in the range from VSSA (VSSB) to VCCA (VCCB). All available ranges are listed in Table 12.

**Table 12. Typical Configuration in Mixed DAC Range Mode**

| Pin | Typical Connection | | Notes |
|---|---|---|---|
| VDD | 4.5V to 5.5V | | |
| VIO | 1.65V to 3.6V | | $V_{IO} \leq V_{DD}$ |
| VCCA, VCCB | Positive output range | $4.5V \leq V_{CC} \leq 11V$ | $V_{SS} \leq V_{DAC} \leq V_{CC}$ |
| | Negative output range | GND | |
| VSSA, VSSB | Positive output range | GND | $V_{SS} \leq V_{DAC} \leq V_{CC}$ |
| | Negative output range | $-11V \leq V_{SS} \leq -4.5V$ | |
| Exposed Pad | GND | | |

In the mixed DAC range mode, when system is power-on reset, the auto-range detector sets the positive DAC groups to default 0V to 5V range; set the negative DAC groups to -10V to 0V range. After power-up, the real output range needs to be configured by software.

## Programming

### Serial Interface Overview

The SGM5207 interface is a 3-wire SPI-compatible interface.

The operation frame is N+2 bytes. Where, N is the number of data bytes to be accessed. The first bit of the frame is W/R (write/read) acknowledge bit. When it's '0', it sets a write operation. When it's '1', it sets a read operation. In a write operation, the data is shifted in on the rising edge of SCLK. In a read operation, the data is shifted out on the falling edge of SCLK.

The access protocol used by the interface is shown in Figure 9.

### Streaming Mode Operation

In stream mode, multiple bytes of data can be written or read in one frame operation. In this mode, a single byte or multiple bytes are accessed which is configured in interface configuration 1 register. And the data to be accessed in increased address sequence or decreased address sequence which is configured by ADDR_ASCEND bit (in interface configuration 0 register).

In stream mode, when the address is increased, if the address 0x7FFF is reached, the next address will loop back to 0x0000. When the address is decreased, if the address 0x0000 is reached, the next address will loop back to 0x7FFF.

The access protocol used in streaming mode is shown in Figure 10.

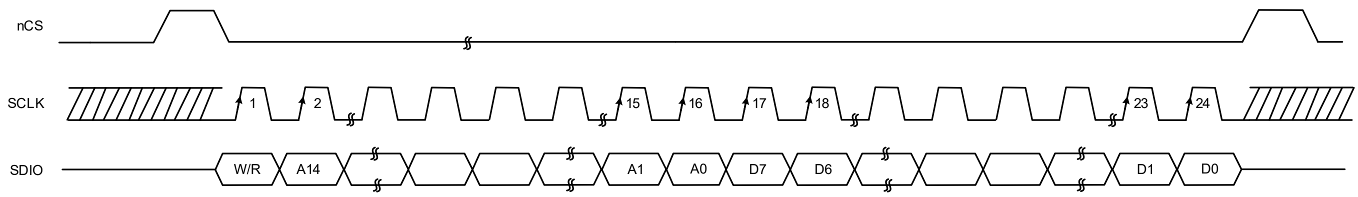



**Figure 9. Serial Interface Write/Read Bus Cycle**

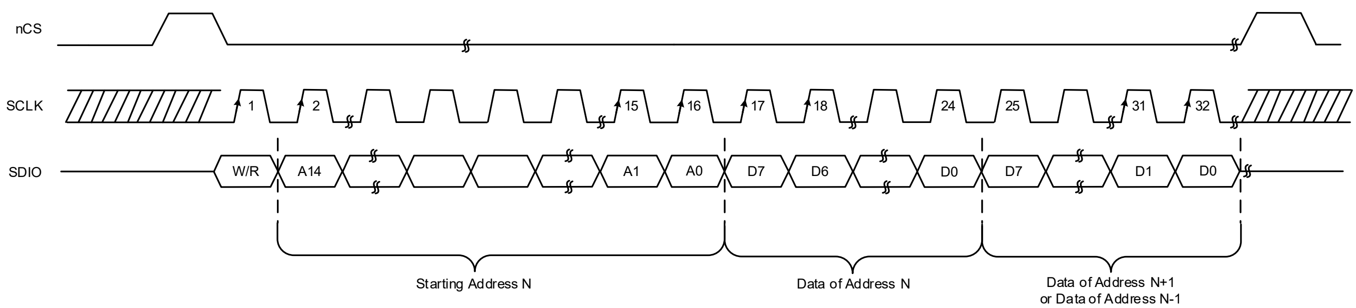



**Figure 10. Serial Interface Streaming Write/Read**

# REGISTER MAPS

R/W: Read/Write bit(s)
R: Read only bit(s)
PORV: Power-On Reset Value

**Table 13. Register Map**

| ADDRESS | TYPE | DEFAULT | REGISTER NAME | | ADDRESS | TYPE | DEFAULT | REGISTER NAME |
|---|---|---|---|---|---|---|---|---|
| 0x00 | R/W | 0x30 | Interface Configuration 0 | | 0x2A | R | 0x00 | ADC5 Data (Low Byte) |
| 0x01 | R/W | 0x00 | Interface Configuration 1 | | 0x2B | R | 0x00 | ADC5 Data (High Byte) |
| 0x02 | R/W | 0x03 | Device Configuration | | 0x2C | R | 0x00 | Internal Temperature Data (Low Byte) |
| 0x03 | R | 0x07 | Device Type | | 0x2D | R | 0x00 | Internal Temperature Data (High Byte) |
| 0x04 | R | 0x07 | Device ID (Low Byte) | | 0x2E | - | - | Reserved |
| 0x05 | R | 0x52 | Device ID (High Byte) | | 0x2F | R/W | 0x08 | Temperature Sensor Conversion Rate |
| 0x06 | R | 0x01 | Version ID | | 0x30 | R/W | 0x00 | DACA0 Data (Low Byte) |
| 0x07 ~ 0x0B | - | - | Reserved | | 0x31 | R/W | 0x00 | DACA0 Data (High Byte) |
| 0x0C | R | 0x51 | Vendor ID (Low Byte) | | 0x32 | R/W | 0x00 | DACA1 Data (Low Byte) |
| 0x0D | R | 0x04 | Vendor ID (High Byte) | | 0x33 | R/W | 0x00 | DACA1 Data (High Byte) |
| 0x0E | - | - | Reserved | | 0x34 | R/W | 0x00 | DACA2 Data (Low Byte) |
| 0x0F | R/W | 0x00 | Register Update | | 0x35 | R/W | 0x00 | DACA2 Data (High Byte) |
| 0x10 | R/W | 0x00 | ADC Configuration | | 0x36 | R/W | 0x00 | DACA3 Data (Low Byte) |
| 0x11 | R/W | 0x61 | False Alarm Configuration | | 0x37 | R/W | 0x00 | DACA3 Data (High Byte) |
| 0x12 | R/W | 0x00 | GPIO Configuration | | 0x38 | R/W | 0x00 | DACA4 Data (Low Byte) |
| 0x13 | R/W | 0xFF | ADC MUX Configuration | | 0x39 | R/W | 0x00 | DACA4 Data (High Byte) |
| 0x14 | R/W | 0x00 | Software Reset | | 0x3A | R/W | 0x00 | DACA5 Data (Low Byte) |
| 0x15 | R/W | 0x00 | DAC Range | | 0x3B | R/W | 0x00 | DACA5 Data (High Byte) |
| 0x16 | R/W | 0x00 | DACA Clear Enable 0 | | 0x3C | R/W | 0x00 | DACA6 Data (Low Byte) |
| 0x17 | R/W | 0x00 | DACA Clear Enable 1 | | 0x3D | R/W | 0x00 | DACA6 Data (High Byte) |
| 0x18 | R/W | 0x00 | DACA Clear Enable 2 | | 0x3E | R/W | 0x00 | DACA7 Data (Low Byte) |
| 0x19 | R/W | 0x00 | DACA Clear Enable 3 | | 0x3F | R/W | 0x00 | DACA7 Data (High Byte) |
| 0x1A | R/W | 0x00 | DACB Clear Enable 0 | | 0x40 | R/W | 0x00 | DACA8 Data (Low Byte) |
| 0x1B | R/W | 0x00 | DACB Clear Enable 1 | | 0x41 | R/W | 0x00 | DACA8 Data (High Byte) |
| 0x1C | R/W | 0x00 | DAC Clear Source 0 | | 0x42 | R/W | 0x00 | DACA9 Data (Low Byte) |
| 0x1D | R/W | 0x00 | DAC Clear Source 1 | | 0x43 | R/W | 0x00 | DACA9 Data (High Byte) |
| 0x1E | R/W | 0x00 | ALARMOUT Source 0 | | 0x44 | R/W | 0x00 | DACA10 Data (Low Byte) |
| 0x1F | R/W | 0x00 | ALARMOUT Source 1 | | 0x45 | R/W | 0x00 | DACA10 Data (High Byte) |
| 0x20 | R | 0x00 | ADC0 Data (Low Byte) | | 0x46 | R/W | 0x00 | DACA11 Data (Low Byte) |
| 0x21 | R | 0x00 | ADC0 Data (High Byte) | | 0x47 | R/W | 0x00 | DACA11 Data (High Byte) |
| 0x22 | R | 0x00 | ADC1 Data (Low Byte) | | 0x48 | R/W | 0x00 | DACA12 Data (Low Byte) |
| 0x23 | R | 0x00 | ADC1 Data (High Byte) | | 0x49 | R/W | 0x00 | DACA12 Data (High Byte) |
| 0x24 | R | 0x00 | ADC2 Data (Low Byte) | | 0x4A | R/W | 0x00 | DACA13 Data (Low Byte) |
| 0x25 | R | 0x00 | ADC2 Data (High Byte) | | 0x4B | R/W | 0x00 | DACA13 Data (High Byte) |
| 0x26 | R | 0x00 | ADC3 Data (Low Byte) | | 0x4C | R/W | 0x00 | DACA14 Data (Low Byte) |
| 0x27 | R | 0x00 | ADC3 Data (High Byte) | | 0x4D | R/W | 0x00 | DACA14 Data (High Byte) |
| 0x28 | R | 0x00 | ADC4 Data (Low Byte) | | 0x4E | R/W | 0x00 | DACA15 Data (Low Byte) |
| 0x29 | R | 0x00 | ADC4 Data (High Byte) | | 0x4F | R/W | 0x00 | DACA15 Data (High Byte) |

## REGISTER MAPS (continued)

**Table 13. Register Map (continued)**

| ADDRESS | TYPE | DEFAULT | REGISTER NAME | | ADDRESS | TYPE | DEFAULT | REGISTER NAME |
|---|---|---|---|---|---|---|---|---|
| 0x50 | R/W | 0x00 | DACA16 Data (Low Byte) | | 0x79 | R/W | 0x00 | DACB4 Data (High Byte) |
| 0x51 | R/W | 0x00 | DACA16 Data (High Byte) | | 0x7A | R/W | 0x00 | DACB5 Data (Low Byte) |
| 0x52 | R/W | 0x00 | DACA17 Data (Low Byte) | | 0x7B | R/W | 0x00 | DACB5 Data (High Byte) |
| 0x53 | R/W | 0x00 | DACA17 Data (High Byte) | | 0x7C | R/W | 0x00 | DACB6 Data (Low Byte) |
| 0x54 | R/W | 0x00 | DACA18 Data (Low Byte) | | 0x7D | R/W | 0x00 | DACB6 Data (High Byte) |
| 0x55 | R/W | 0x00 | DACA18 Data (High Byte) | | 0x7E | R/W | 0x00 | DACB7 Data (Low Byte) |
| 0x56 | R/W | 0x00 | DACA19 Data (Low Byte) | | 0x7F | R/W | 0x00 | DACB7 Data (High Byte) |
| 0x57 | R/W | 0x00 | DACA19 Data (High Byte) | | 0x80 | R/W | 0x00 | DACB8 Data (Low Byte) |
| 0x58 | R/W | 0x00 | DACA20 Data (Low Byte) | | 0x81 | R/W | 0x00 | DACB8 Data (High Byte) |
| 0x59 | R/W | 0x00 | DACA20 Data (High Byte) | | 0x82 | R/W | 0x00 | DACB9 Data (Low Byte) |
| 0x5A | R/W | 0x00 | DACA21 Data (Low Byte) | | 0x83 | R/W | 0x00 | DACB9 Data (High Byte) |
| 0x5B | R/W | 0x00 | DACA21 Data (High Byte) | | 0x84 | R/W | 0x00 | DACB10 Data (Low Byte) |
| 0x5C | R/W | 0x00 | DACA22 Data (Low Byte) | | 0x85 | R/W | 0x00 | DACB10 Data (High Byte) |
| 0x5D | R/W | 0x00 | DACA22 Data (High Byte) | | 0x86 | R/W | 0x00 | DACB11 Data (Low Byte) |
| 0x5E | R/W | 0x00 | DACA23 Data (Low Byte) | | 0x87 | R/W | 0x00 | DACB11 Data (High Byte) |
| 0x5F | R/W | 0x00 | DACA23 Data (High Byte) | | 0x88 | R/W | 0x00 | DACB12 Data (Low Byte) |
| 0x60 | R/W | 0x00 | DACA24 Data (Low Byte) | | 0x89 | R/W | 0x00 | DACB12 Data (High Byte) |
| 0x61 | R/W | 0x00 | DACA24 Data (High Byte) | | 0x8A | R/W | 0x00 | DACB13 Data (Low Byte) |
| 0x62 | R/W | 0x00 | DACA25 Data (Low Byte) | | 0x8B | R/W | 0x00 | DACB13 Data (High Byte) |
| 0x63 | R/W | 0x00 | DACA25 Data (High Byte) | | 0x8C | R/W | 0x00 | DACB14 Data (Low Byte) |
| 0x64 | R/W | 0x00 | DACA26 Data (Low Byte) | | 0x8D | R/W | 0x00 | DACB14 Data (High Byte) |
| 0x65 | R/W | 0x00 | DACA26 Data (High Byte) | | 0x8E | R/W | 0x00 | DACB15 Data (Low Byte) |
| 0x66 | R/W | 0x00 | DACA27 Data (Low Byte) | | 0x8F | R/W | 0x00 | DACB15 Data (High Byte) |
| 0x67 | R/W | 0x00 | DACA27 Data (High Byte) | | 0x90 | R | 0x00 | Alarm Status 0 |
| 0x68 | R/W | 0x00 | DACA28 Data (Low Byte) | | 0x91 | R | 0x00 | Alarm Status 1 |
| 0x69 | R/W | 0x00 | DACA28 Data (High Byte) | | 0x92 | R | 0x00 | General Status |
| 0x6A | R/W | 0x00 | DACA29 Data (Low Byte) | | 0x93 ~ 0x99 | - | - | Reserved |
| 0x6B | R/W | 0x00 | DACA29 Data (High Byte) | | 0x9A | R/W | 0x3F | GPIO |
| 0x6C | R/W | 0x00 | DACA30 Data (Low Byte) | | 0x9B ~ 0x9D | - | - | Reserved |
| 0x6D | R/W | 0x00 | DACA30 Data (High Byte) | | 0x9E | R/W | 0x00 | DAC Broadcast Data (Low byte) |
| 0x6E | R/W | 0x00 | DACA31 Data (Low Byte) | | 0x9F | R/W | 0x00 | DAC Broadcast Data (High byte) |
| 0x6F | R/W | 0x00 | DACA31 Data (High Byte) | | 0xA0 | R/W | 0xFF | Internal Temperature High Limit |
| 0x70 | R/W | 0x00 | DACB0 Data (Low Byte) | | 0xA1 | R/W | 0x00 | Internal Temperature Low Limit |
| 0x71 | R/W | 0x00 | DACB0 Data (High Byte) | | 0xA2 | R/W | 0xFF | Thermal Alarm High Limit |
| 0x72 | R/W | 0x00 | DACB1 Data (Low Byte) | | 0xA3 | - | - | Reserved |
| 0x73 | R/W | 0x00 | DACB1 Data (High Byte) | | 0xA4 | R/W | 0xFF | ADC0 High Limit (Low Byte) |
| 0x74 | R/W | 0x00 | DACB2 Data (Low Byte) | | 0xA5 | R/W | 0x0F | ADC0 High Limit (High Byte) |
| 0x75 | R/W | 0x00 | DACB2 Data (High Byte) | | 0xA6 | R/W | 0x00 | ADC0 Low Limit (Low Byte) |
| 0x76 | R/W | 0x00 | DACB3 Data (Low Byte) | | 0xA7 | R/W | 0x00 | ADC0 Low Limit (High Byte) |
| 0x77 | R/W | 0x00 | DACB3 Data (High Byte) | | 0xA8 | R/W | 0xFF | ADC1 High Limit (Low Byte) |
| 0x78 | R/W | 0x00 | DACB4 Data (Low Byte) | | 0xA9 | R/W | 0x0F | ADC1 High Limit (High Byte) |

## REGISTER MAPS (continued)

**Table 13. Register Map (continued)**

| ADDRESS | TYPE | DEFAULT | REGISTER NAME | | ADDRESS | TYPE | DEFAULT | REGISTER NAME |
|---|---|---|---|---|---|---|---|---|
| 0xAA | R/W | 0x00 | ADC1 Low Limit (Low Byte) | | 0xCE | R/W | 0x00 | DACB Clear 0 |
| 0xAB | R/W | 0x00 | ADC1 Low Limit (High Byte) | | 0xCF | R/W | 0x00 | DACB Clear 1 |
| 0xAC | R/W | 0xFF | ADC2 High Limit (Low Byte) | | 0xD0 | R/W | 0x00 | DACA Power-Down 0 |
| 0xAD | R/W | 0x0F | ADC2 High Limit (High Byte) | | 0xD1 | R/W | 0x00 | DACA Power-Down 1 |
| 0xAE | R/W | 0x00 | ADC2 Low Limit (Low Byte) | | 0xD2 | R/W | 0x00 | DACA Power-Down 2 |
| 0xAF | R/W | 0x00 | ADC2 Low Limit (High Byte) | | 0xD3 | R/W | 0x00 | DACA Power-Down 3 |
| 0xB0 | R/W | 0xFF | ADC3 High Limit (Low Byte) | | 0xD4 | R/W | 0x00 | DACB Power-Down 0 |
| 0xB1 | R/W | 0x0F | ADC3 High Limit (High Byte) | | 0xD5 | R/W | 0x00 | DACB Power-Down 1 |
| 0xB2 | R/W | 0x00 | ADC3 Low Limit (Low Byte) | | 0xD6 | R/W | 0x00 | Monitor Power Enable |
| 0xB3 | R/W | 0x00 | ADC3 Low Limit (High Byte) | | 0xD7 ~ 0xDF | - | - | Reserved |
| 0xB4 | R/W | 0xFF | ADC4 High Limit (Low Byte) | | 0xE0 | R/W | 0x00 | ADC Trigger |
| 0xB5 | R/W | 0x0F | ADC4 High Limit (High Byte) | | All others | - | - | Reserved |
| 0xB6 | R/W | 0x00 | ADC4 Low Limit (Low Byte) | | | | | |
| 0xB7 | R/W | 0x00 | ADC4 Low Limit (High Byte) | | | | | |
| 0xB8 | R/W | 0xFF | ADC5 High Limit (Low Byte) | | | | | |
| 0xB9 | R/W | 0x0F | ADC5 High Limit (High Byte) | | | | | |
| 0xBA | R/W | 0x00 | ADC5 Low Limit (Low Byte) | | | | | |
| 0xBB | R/W | 0x00 | ADC5 Low Limit (High Byte) | | | | | |
| 0xBC ~ 0xBF | - | - | Reserved | | | | | |
| 0xC0 | R/W | 0x0A | Thermal Alarm Hysteresis | | | | | |
| 0xC1 | R/W | 0x08 | ADC0 Hysteresis | | | | | |
| 0xC2 | R/W | 0x08 | ADC1 Hysteresis | | | | | |
| 0xC3 | R/W | 0x08 | ADC2 Hysteresis | | | | | |
| 0xC4 | R/W | 0x08 | ADC3 Hysteresis | | | | | |
| 0xC5 | R/W | 0x08 | ADC4 Hysteresis | | | | | |
| 0xC6 | R/W | 0x08 | ADC5 Hysteresis | | | | | |
| 0xC7 ~ 0xC9 | - | - | Reserved | | | | | |
| 0xCA | R/W | 0x00 | DACA Clear 0 | | | | | |
| 0xCB | R/W | 0x00 | DACA Clear 1 | | | | | |
| 0xCC | R/W | 0x00 | DACA Clear 2 | | | | | |
| 0xCD | R/W | 0x00 | DACA Clear 3 | | | | | |

# REGISTER MAPS (continued)

## Interface Configuration 0 Register

Register address: 0x00

Reset value = 0x30

**Table 14. Interface Configuration 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | REG_RESET | Register Reset (Self-Clearing)<br>0 = No action (default)<br>1 = Reset. All registers are reset except address 0x00, 0x01 | | 0 | R/W |
| D[6] | Reserved | | | 0 | R/W |
| D[5] | ADDR_ASCEND | Address Ascend<br>0 = Descend. Address is decreased while streaming operation<br>1 = Ascend. Address is increased while streaming operation (default) | | 1 | R/W |
| D[4] | Reserved | | | 1 | R/W |
| D[3:0] | Reserved | | | 0000 | R/W |

NOTES:
1. This register is not reset by SOFT_RESET[7:0].
2. This register doesn't require update (address 0x0F).

## Interface Configuration 1 Register

Register address: 0x01

Reset value = 0x00

**Table 15. Interface Configuration 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | SINGLE_INSTR | Single Instruction Enable<br>0 = Streaming mode (default)<br>1 = Single instruction | | 0 | R/W |
| D[6] | Reserved | | | 0 | R/W |
| D[5] | READBACK | Read Back<br>0 = DAC read back from active registers (default)<br>1 = DAC read back from buffer registers | | 0 | R/W |
| D[4:0] | Reserved | | | 00000 | R/W |

NOTES:
1. This register is not reset by SOFT_RESET[7:0].
2. This register doesn't require update (address 0x0F).

# REGISTER MAPS (continued)

## Device Configuration Register

Register address: 0x02

Reset value = 0x03

**Table 16. Device Configuration Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:2] | Reserved | | | 000000 | R/W |
| D[1:0] | POWER_MODE[1:0] | Mode<br>00 = Normal mode, full power and full performance<br>01 = Reserved<br>10 = Reserved<br>11 = Power-down mode, lowest power, only SPI active (default) | Overwrite the power enable registers in one operation. | 11 | R/W |

## Device Type Register

Register address: 0x03

Reset value = 0x07

**Table 17. Device Type Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R |
| D[3:0] | DEVICE_TYPE[3:0] | Identifies the device as a precision analog monitor and control. | | 0111 | R |

## Device ID (Low Byte) Register

Register address: 0x04

Reset value = 0x07

**Table 18. Device ID (Low Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | DEVICE_ID[7:0] | Device ID. Low byte. | | 00000111 | R |

## Device ID (High Byte) Register

Register address: 0x05

Reset value = 0x52

**Table 19. Chip ID (High Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | DEVICE_ID[15:8] | Device ID. High byte. | | 01010010 | R |

# REGISTER MAPS (continued)

## Version ID Register

Register address: 0x06

Reset value = 0x01

**Table 20. Version ID Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | VERSION_ID[7:0] | Version ID. | | 00000001 | R |

## Vendor ID (Low Byte) Register

Register address: 0x0C

Reset value = 0x51

**Table 21. Vendor ID (Low Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | VENDOR_ID[7:0] | Vendor ID. Low byte. | | 01010001 | R |

## Vendor ID (High Byte) Register

Register address: 0x0D

Reset value = 0x04

**Table 22. Vendor ID (High Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | VENDOR_ID[15:8] | Vendor ID. High byte. | | 00000100 | R |

## Register Update Register

Register address: 0x0F

Reset value = 0x00

**Table 23. Register Update Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:6] | Reserved | | | 00 | R/W |
| D[5] | LT_UPDATE | When it's enabled by setting it to '1', the chip updates the internal temperature data registers. | | 0 | R/W |
| D[4] | ADC_UPDATE | When it's enabled by setting it to '1', the chip updates the ADC data registers. | The function is used when running the ADC in auto mode. | 0 | R/W |
| D[3:1] | Reserved | | | 000 | R/W |
| D[0] | DAC_UPDATE | When it's enabled by setting it to '1', DAC data is transferred from DAC buffer registers to DAC active registers by the chip. | | 0 | R/W |

# REGISTER MAPS (continued)

## ADC Configuration Register

Register address: 0x10

Reset value = 0x00

**Table 24 ADC Configuration Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | CMODE | ADC Conversion Mode Bit<br>0 = Direct mode (default)<br>1 = Auto mode | The bit configures the ADC conversion mode. | 0 | R/W |
| D[6:5] | CONV_RATE[1:0] | ADC Conversion Rate | Refer to Table 25. | 00 | R/W |
| D[4] | ADC_RANGE | ADC Range Selection Bit<br>0 = 0V to 5V range (default)<br>1 = 0V to 2.5V range | | 0 | R/W |
| D[3] | ADC_CAL | When it's enabled by setting it to '1', the chip will complete the offset calibration sequence upon ADC conversion trigger. | | 0 | R/W |
| D[2] | Reserved | | | 0 | R/W |
| D[1] | SDOZDD | When it's enabled by setting it to '1', high impedance-to-driven delay increase for SDIO pin.<br>Increasing the delay of the SDIO high impedance to active by 2ns. | | 0 | R/W |
| D[0] | Reserved | | | 0 | R/W |

**Table 25. CONV_RATE[1:0] Bits Configuration**

| CONV_RATE[1:0] | Acquisition Time (μs) | Conversion Time (μs) | Throughput (kSPS) (Single-Channel, Auto Mode) |
|---|---|---|---|
| 00 (default) | 2.125 | 1.875 | 250 |
| 01 | 2.125 | 1.875 | 250 |
| 10 | 6.125 | 1.875 | 125 |
| 11 | 30.125 | 1.875 | 31.25 |

# REGISTER MAPS (continued)

## False Alarm Configuration Register

Register address: 0x11

Reset value = 0x61

**Table 26. False Alarm Configuration Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:5] | ADC_FALR[2:0] | False Alarm Protection for ADC Channels | Refer to Table 27. | 011 | R/W |
| D[4] | Reserved | | | 0 | R/W |
| D[3:1] | LT_FALR[2:0] | False Alarm Protection for Temperature Sensor | Refer to Table 28. | 000 | R/W |
| D[0] | Reserved | | | 1 | R/W |

**Table 27. ADC_FALR[2:0] Bits Configuration**

| ADC_FALR[2:0] | N Consecutive Samples before Alarm is Set |
|---|---|
| 000 | 1 |
| 001 | 4 |
| 010 | 8 |
| 011 (default) | 16 |
| 100 | 32 |
| 101 | 64 |
| 110 | 128 |
| 111 | 256 |

**Table 28. LT_FALR[2:0] Bits Configuration**

| LT_FALR[2:0] | N Consecutive Samples before Alarm is Set |
|---|---|
| 000 (default) | 1 |
| 001 | 2 |
| 011 | 3 |
| 111 | 4 |
| All others | 1 |

# REGISTER MAPS (continued)

## GPIO Configuration Register

Register address: 0x12

Reset value = 0x00

**Table 29. GPIO Configuration Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:6] | Reserved | | | 00 | R/W |
| D[5] | ALMIN_EN | nALARMIN Pin Enable<br>0 = GPIO5 operation (default)<br>1 = nALARMIN operation | | 0 | R/W |
| D[4] | DAV_EN | nDAV Pin Enable<br>0 = GPIO4 operation (default)<br>1 = nDAV operation | | 0 | R/W |
| D[3] | ADCTRIG_EN | nADCTRIG Pin Enable<br>0 = GPIO3 operation (default)<br>1 = nADCTRIG operation | | 0 | R/W |
| D[2] | ALMOUT_EN | nALARMOUT Pin Enable<br>0 = GPIO2 operation (default)<br>1 = nALARMOUT operation | | 0 | R/W |
| D[1] | CLEARB_EN | nCLEARB Pin Enable<br>0 = GPIO1 operation (default)<br>1 = nCLEARB operation | | 0 | R/W |
| D[0] | CLEARA_EN | nCLEARA Pin Enable<br>0 = GPIO0 operation (default)<br>1 = nCLEARA operation | | 0 | R/W |

## ADC MUX Configuration Register

Register address: 0x13

Reset value = 0xFF

**Table 30. ADC MUX Configuration Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:6] | Reserved | | | 11 | R/W |
| D[5] | ADC5_EN | When corresponding bit is set to '1', the corresponding analog input channel ADCn/GPIOn is used as an ADC input and will be accessed during an ADC conversion cycle. Ignore the corresponding setting in the GPIO configuration register and block the alternative function.<br>When corresponding bit is cleared to '0', the corresponding input channel ADCn/GPIOn is used as a GPIO and will be ignored during an ADC conversion cycle. The corresponding bit in the GPIO configuration register is valid. | | 1 | R/W |
| D[4] | ADC4_EN | | | 1 | R/W |
| D[3] | ADC3_EN | | | 1 | R/W |
| D[2] | ADC2_EN | | | 1 | R/W |
| D[1] | ADC1_EN | | | 1 | R/W |
| D[0] | ADC0_EN | | | 1 | R/W |

## Software Reset Register

Register address: 0x14

Reset value = 0x00

**Table 31. Software Reset Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | SOFT_RESET[7:0] | When writing key word 0xAD to the register, it triggers a reset event.<br>All registers are reset to their default values. | | 00000000 | R/W |

# REGISTER MAPS (continued)

## DAC Range Register

Register address: 0x15

Reset value = 0x00

**Table 32. DAC Range Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB_LC | When it's set to '1', enable low-current mode of the DACs for group B. | | 0 | R/W |
| D[6:4] | DACB_RANGE[2:0] | Configure DAC group B output voltage range. | Overrides output range which is set by the auto-range detection circuit (the auto-range is set when the chip is reset by power-up). The detailed settings refer to Table 33. | 000 | R/W |
| D[3] | DACA_LC | When it's set to '1', enable low-current mode of the DACs for group A. | | 0 | R/W |
| D[2:0] | DACA_RANGE[2:0] | Configure DAC group A output voltage range. | Overrides output range which is set by the auto-range detection circuit (the auto-range is set when the chip is reset by power-up). The detailed settings refer to Table 33. | 000 | R/W |

**Table 33. DACn_RANGE[2:0] Bits Configuration**

| DACn_RANGE[2:0] | DAC Group Output Voltage Range |
|---|---|
| 0xx | Range set by auto-range detection circuit |
| 100 | -10V to 0V |
| 101 | -5V to 0V |
| 110 | 0V to 10V |
| 111 | 0V to 5V |

# REGISTER MAPS (continued)

## DACA Clear Enable 0 Register

Register address: 0x16

Reset value = 0x00

**Table 34. DACA Clear Enable 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA7_CLREN | 0 = DAC_An state is not affected by a clear event (default)<br>1 = DAC_An passively enters into a clear state with a clear event<br>When corresponding bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected. | | 0 | R/W |
| D[6] | DACA6_CLREN | | | 0 | R/W |
| D[5] | DACA5_CLREN | | | 0 | R/W |
| D[4] | DACA4_CLREN | | | 0 | R/W |
| D[3] | DACA3_CLREN | | | 0 | R/W |
| D[2] | DACA2_CLREN | | | 0 | R/W |
| D[1] | DACA1_CLREN | | | 0 | R/W |
| D[0] | DACA0_CLREN | | | 0 | R/W |

## DACA Clear Enable 1 Register

Register address: 0x17

Reset value = 0x00

**Table 35. DACA Clear Enable 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA15_CLREN | 0 = DAC_An state is not affected by a clear event (default)<br>1 = DAC_An passively enters into a clear state with a clear event<br>When corresponding bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected. | | 0 | R/W |
| D[6] | DACA14_CLREN | | | 0 | R/W |
| D[5] | DACA13_CLREN | | | 0 | R/W |
| D[4] | DACA12_CLREN | | | 0 | R/W |
| D[3] | DACA11_CLREN | | | 0 | R/W |
| D[2] | DACA10_CLREN | | | 0 | R/W |
| D[1] | DACA9_CLREN | | | 0 | R/W |
| D[0] | DACA8_CLREN | | | 0 | R/W |

# REGISTER MAPS (continued)

## DACA Clear Enable 2 Register

Register address: 0x18

Reset value = 0x00

**Table 36. DACA Clear Enable 2 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA23_CLREN | 0 = DAC_An state is not affected by a clear event (default)<br>1 = DAC_An passively enters into a clear state with a clear event<br>When corresponding bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected. | | 0 | R/W |
| D[6] | DACA22_CLREN | | | 0 | R/W |
| D[5] | DACA21_CLREN | | | 0 | R/W |
| D[4] | DACA20_CLREN | | | 0 | R/W |
| D[3] | DACA19_CLREN | | | 0 | R/W |
| D[2] | DACA18_CLREN | | | 0 | R/W |
| D[1] | DACA17_CLREN | | | 0 | R/W |
| D[0] | DACA16_CLREN | | | 0 | R/W |

## DACA Clear Enable 3 Register

Register address: 0x19

Reset value = 0x00

**Table 37. DACA Clear Enable 3 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA31_CLREN | 0 = DAC_An state is not affected by a clear event (default)<br>1 = DAC_An passively enters into a clear state with a clear event<br>When corresponding bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected. | | 0 | R/W |
| D[6] | DACA30_CLREN | | | 0 | R/W |
| D[5] | DACA29_CLREN | | | 0 | R/W |
| D[4] | DACA28_CLREN | | | 0 | R/W |
| D[3] | DACA27_CLREN | | | 0 | R/W |
| D[2] | DACA26_CLREN | | | 0 | R/W |
| D[1] | DACA25_CLREN | | | 0 | R/W |
| D[0] | DACA24_CLREN | | | 0 | R/W |

# REGISTER MAPS (continued)

## DACB Clear Enable 0 Register

Register address: 0x1A

Reset value = 0x00

**Table 38. DACB Clear Enable 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB7_CLREN | 0 = DAC_Bn state is not affected by a clear event (default)<br>1 = DAC_Bn passively enters into a clear state with a clear event<br>When corresponding bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected. | | 0 | R/W |
| D[6] | DACB6_CLREN | | | 0 | R/W |
| D[5] | DACB5_CLREN | | | 0 | R/W |
| D[4] | DACB4_CLREN | | | 0 | R/W |
| D[3] | DACB3_CLREN | | | 0 | R/W |
| D[2] | DACB2_CLREN | | | 0 | R/W |
| D[1] | DACB1_CLREN | | | 0 | R/W |
| D[0] | DACB0_CLREN | | | 0 | R/W |

## DACB Clear Enable 1 Register

Register address: 0x1B

Reset value = 0x00

**Table 39. DACB Clear Enable 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB15_CLREN | 0 = A DAC_Bn state is not affected by a clear event (default)<br>1 = DAC_Bn passively enters into a clear state with a clear event<br>When corresponding bit is set to '1', the corresponding DAC channel will go into clear state when a clear event is detected. | | 0 | R/W |
| D[6] | DACB14_CLREN | | | 0 | R/W |
| D[5] | DACB13_CLREN | | | 0 | R/W |
| D[4] | DACB12_CLREN | | | 0 | R/W |
| D[3] | DACB11_CLREN | | | 0 | R/W |
| D[2] | DACB10_CLREN | | | 0 | R/W |
| D[1] | DACB9_CLREN | | | 0 | R/W |
| D[0] | DACB8_CLREN | | | 0 | R/W |

# REGISTER MAPS (continued)

## DAC Clear Source 0 Register

Register address: 0x1C

Reset value = 0x00

**Table 40. DAC Clear Source 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | REF_ALR_CLR | When the corresponding bit is set to '1', the corresponding alarm will be one of sources to force DACs into a clear state.<br>At the same time, in order to bring DAC_n into clear mode, make sure that DAC_n is enabled in the DAC clear enable registers. | | 0 | R/W |
| D[6] | ALMIN_ALR_CLR | | | 0 | R/W |
| D[5] | ADC5_ALR_CLR | | | 0 | R/W |
| D[4] | ADC4_ALR_CLR | | | 0 | R/W |
| D[3] | ADC3_ALR_CLR | | | 0 | R/W |
| D[2] | ADC2_ALR_CLR | | | 0 | R/W |
| D[1] | ADC1_ALR_CLR | | | 0 | R/W |
| D[0] | ADC0_ALR_CLR | | | 0 | R/W |

## DAC Clear Source 1 Register

Register address: 0x1D

Reset value = 0x00

**Table 41. DAC Clear Source 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:3] | Reserved | | | 00000 | R/W |
| D[2] | THERM_ALR_CLR | When the corresponding bit is set to '1', the corresponding alarm will be one of sources to force DACs into a clear state.<br>At the same time, in order to bring DAC_n into clear mode, make sure that DAC_n is enabled in the DAC clear enable registers. | | 0 | R/W |
| D[1] | LTHIGH_ALR_CLR | | | 0 | R/W |
| D[0] | LTLOW_ALR_CLR | | | 0 | R/W |

# REGISTER MAPS (continued)

## ALARMOUT Source 0 Register

Register address: 0x1E

Reset value = 0x00

**Table 42. ALARMOUT Source 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | REF_ALR_OUT | When corresponding bit is set to '1', the corresponding alarm will be one of sources to activate the nALARMOUT pin.<br>The nALARMOUT pin must be enabled in GPIO configuration register at the same time. | | 0 | R/W |
| D[6] | ALMIN_ALR_OUT | | | 0 | R/W |
| D[5] | ADC5_ALR_OUT | | | 0 | R/W |
| D[4] | ADC4_ALR_OUT | | | 0 | R/W |
| D[3] | ADC3_ALR_OUT | | | 0 | R/W |
| D[2] | ADC2_ALR_OUT | | | 0 | R/W |
| D[1] | ADC1_ALR_OUT | | | 0 | R/W |
| D[0] | ADC0_ALR_OUT | | | 0 | R/W |

## ALARMOUT Source 1 Register

Register address: 0x1F

Reset value = 0x00

**Table 43. ALARMOUT Source 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3] | ALARM_LATCH_DIS | Alarm Latch Enable/Disable Bit<br>0 = Alarm bits latch enabled. When an alarm bit is set to '1', the bit only can be cleared by reading the alarm register. And if the alarm condition is not disappeared; the bit will be set again (default)<br>1 = Alarm bits are not latched. An alarm bit is set to '1' if an alarm limit is exceeded. And the alarm bit is cleared automatically if the alarm trigger condition disappeared | | 0 | R/W |
| D[2] | THERM_ALR_OUT | The according bits select the alarms sources which ones can active the nALARMOUT pin.<br>The nALARMOUT pin must be enabled in GPIO configuration register at the same time. | | 0 | R/W |
| D[1] | LTHIGH_ALR_OUT | | | 0 | R/W |
| D[0] | LTLOW_ALR_OUT | | | 0 | R/W |

# REGISTER MAPS (continued)

## ADCn Data (Low Byte) Registers

Register address: 0x20 to 0x2B

Reset value = 0x00

**Table 44. ADCn Data (Low Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | ADCn_DATA[7:0] | Stores the low byte of the 12-bit ADC_n conversion results. | | 00000000 | R |

## ADCn Data (High Byte) Registers

Register address: 0x20 to 0x2B

Reset value = 0x00

**Table 45. ADCn Data (High Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R |
| D[3:0] | ADCn_DATA [11:8] | Stores the high byte of the 12-bit ADC_n conversion results. | | 0000 | R |

## Internal Temperature Data (Low Byte) Register

Register address: 0x2C

Reset value = 0x00

**Table 46. Internal Temperature Data (Low Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | LT_DATA[3:0] | Stores the fractional data of the temperature sensor. | | 0000 | R |
| D[3:0] | Reserved | | | 0000 | R |

## Internal Temperature Data (High Byte) Register

Register address: 0x2D

Reset value = 0x00

**Table 47. Internal Temperature Data (High Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | LT_DATA[11:4] | Stores the integral data of the temperature sensor. | | 00000000 | R |

## Temperature Sensor Conversion Rate Register

Register address: 0x2F

Reset value = 0x08

**Table 48. Temperature Sensor Conversion Rate Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3:0] | LT_CONV_RATE[3:0] | Stores the settings of temperature sensor conversion rate. | | 1000 | R/W |

# REGISTER MAPS (continued)

## DAC Group A Configuration: DACAn Data (Low Byte) Registers

Register address: 0x30 to 0x6F

Reset value = 0x00

**Table 49. DACAn Data (Low Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | DACAn_DATA[7:0] | Stores the low byte of the 12-bit data to be loaded to the DAC_An. | | 00000000 | R/W |

## DAC Group A Configuration: DACAn Data (High Byte) Registers

Register address: 0x30 to 0x6F

Reset value = 0x00

**Table 50. DACAn Data (High Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3:0] | DACAn_DATA[11:8] | Stores the high byte of the 12-bit data to be loaded to the DAC_An. | | 0000 | R/W |

## DAC Group B Configuration: DACBn Data (Low Byte) Registers

Register address: 0x70 to 0x8F

Reset value = 0x00

**Table 51. DACBn Data (Low Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | DACBn_DATA[7:0] | Stores the low byte of the 12-bit data to be loaded to the DAC_Bn. | | 00000000 | R/W |

## DAC Group B Configuration: DACBn Data (High Byte) Registers

Register address: 0x70 to 0x8F

Reset value = 0x00

**Table 52. DACBn Data (High Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3:0] | DACBn_DATA[11:8] | Stores the high byte of the 12-bit data to be loaded to the DAC_Bn. | | 0000 | R/W |

# REGISTER MAPS (continued)

## Alarm Status 0 Register

Register address: 0x90

Reset value = 0x00

**Table 53. Alarm Status 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | REF_ALR | 1 = When the internal reference voltage is lower than 2.2V | | 0 | R |
| D[6] | ALMIN_ALR | 1 = When the nALARMIN pin is enabled and set low | | 0 | R |
| D[5] | ADC5_ALR | 1 = When ADC5 exceeds the limitation defined by the corresponding threshold registers | | 0 | R |
| D[4] | ADC4_ALR | 1 = When ADC4 exceeds the limitation defined by the corresponding threshold registers | | 0 | R |
| D[3] | ADC3_ALR | 1 = When ADC3 exceeds the limitation defined by the corresponding threshold registers | | 0 | R |
| D[2] | ADC2_ALR | 1 = When ADC2 exceeds the limitation defined by the corresponding threshold registers | | 0 | R |
| D[1] | ADC1_ALR | 1 = When ADC1 exceeds the limitation defined by the corresponding threshold registers | | 0 | R |
| D[0] | ADC0_ALR | 1 = When ADC0 exceeds the limitation defined by the corresponding threshold registers | | 0 | R |

## Alarm Status 1 Register

Register address: 0x91

Reset value = 0x00

**Table 54. Alarm Status 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:3] | Reserved | | | 00000 | R |
| D[2] | THERM_ALR | Over-Temperature Thermal Alarm Flag<br>1 = When the die temperature is equal to or higher than the thermal threshold | | 0 | R |
| D[1] | LTHIGH_ALR | 1 = When the temperature sensor exceeds the limitation defined by the upper threshold | | 0 | R |
| D[0] | LTLOW_ALR | 1 = When the temperature sensor exceeds the limitation defined by the lower threshold | | 0 | R |

# REGISTER MAPS (continued)

## General Status Register

Register address: 0x92

Reset value = 0x00

**Table 55. General Status Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | VCCB | It's status indicator of VCC of DAC group B. | | 0 | R |
| D[6] | VCCA | It's status indicator of VCC of DAC group A. | | 0 | R |
| D[5] | VSSB | It's status indicator of VSS of DAC group B. | | 0 | R |
| D[4] | VSSA | It's status indicator of VSS of DAC group A. | | 0 | R |
| D[3] | ADC_READY | ADC Ready Indicator<br>ADC_READY = 1 means ADC is ready to be triggered and start converting.<br>When power-up or reset, ADC_READY remains '0' until ADC_EN is set to '1' and ADC channel is enabled.<br>During ADC conversion, ADC_READY keeps '0'.<br>During ADC configuration sequence which will stop ADC, ADC_READY keeps '0'. | | 0 | R |
| D[2] | LT_BUSY | Internal Temperature Sensor ADC Status Indicator<br>0 = Temperature sensor ADC is idle (default)<br>1 = Temperature sensor ADC is converting | | 0 | R |
| D[1] | GALR | Global Alarm Bit<br>Any of the alarm bits setting will cause this bit to be set to '1'.<br>This bit only can be cleared by reading the alarm status register. | | 0 | R |
| D[0] | DAVF | ADC Data Available Flag Bit<br>Direct mode only. Keeps '0' in auto mode.<br>0 = ADC is converting (default)<br>1 = ADC data is ready | | 0 | R |

## GPIO Register

Register address: 0x9A

Reset value = 0x3F

**Table 56. GPIO Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:6] | Reserved | | | 00 | R/W |
| D[5] | GPIO5 | When the GPIO pin is used output, writing '1' will set the pin to high impedance. Writing '0' will set the pin to logic low.<br>Whether the GPIO pin is used as output or input, a read operation will get the status of the GPIO pin.<br>The GPIO pin is reset to high-impedance default. | | 1 | R/W |
| D[4] | GPIO4 | | | 1 | R/W |
| D[3] | GPIO3 | | | 1 | R/W |
| D[2] | GPIO2 | | | 1 | R/W |
| D[1] | GPIO1 | | | 1 | R/W |
| D[0] | GPIO0 | | | 1 | R/W |

## REGISTER MAPS (continued)

### DAC Broadcast Data (Low Byte) Register

Register address: 0x9E

Reset value = 0x00

**Table 57. DAC Broadcast Data (Low Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | DAC_BRDCAST_DATA[7:0] | The data sets all DACn_Data low byte buffers. | | 00000000 | R/W |

### DAC Broadcast Data (High Byte) Register

Register address: 0x9F

Reset value = 0x00

**Table 58. DAC Broadcast Data (High Byte) Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3:0] | DAC_BRDCAST_DATA[11:8] | The data sets all DACn_Data high byte buffers. | | 0000 | R/W |

### Internal Temperature High Limit Register

Register address: 0xA0

Reset value = 0xFF

**Table 59. Internal Temperature High Limit Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | LT_HL[7:0] | Sets the high temperature limit. 1℃ resolution. | | 11111111 | R/W |

### Internal Temperature Low Limit Register

Register address: 0xA1

Reset value = 0x00

**Table 60. Internal Temperature Low Limit Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | LT_LL[7:0] | Sets the low temperature limit. 1℃ resolution. | | 00000000 | R/W |

### Thermal Alarm High Limit Register

Register address: 0xA2

Reset value = 0xFF

**Table 61. Thermal Alarm High Limit Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | THERM_HL[7:0] | Sets the over-temperature limit. 1℃ resolution. | | 11111111 | R/W |

# REGISTER MAPS (continued)

## ADCn High Limit (Low Byte) Registers

Register address: 0xA4 to 0xBB

Reset value = 0xFF

**Table 62. ADCn High Limit (Low Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | ADCn_HL[7:0] | Sets the low byte of 12-bit upper threshold for the ADCn channel. | | 11111111 | R/W |

## ADCn High Limit (High Byte) Registers

Register address: 0xA4 to 0xBB

Reset value = 0x0F

**Table 63. ADCn High Limit (High Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3:0] | ADCn_HL[11:8] | Sets the high byte of 12-bit upper threshold for the ADCn channel. | | 1111 | R/W |

## ADCn Low Limit (Low Byte) Registers

Register address: 0xA4 to 0xBB

Reset value = 0x00

**Table 64. ADCn Low Limit (Low Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | ADCn_LL[7:0] | Sets the low byte of 12-bit lower threshold for the ADCn channel. | | 00000000 | R/W |

## ADCn Low Limit (High Byte) Registers

Register address: 0xA4 to 0xBB

Reset value = 0x00

**Table 65. ADCn Low Limit (High Byte) Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:4] | Reserved | | | 0000 | R/W |
| D[3:0] | ADCn_LL[11:8] | Sets the high byte of 12-bit lower threshold for ADCn channel. | | 0000 | R/W |

# REGISTER MAPS (continued)

## Thermal Alarm Hysteresis Register

Register address: 0xC0

Reset value = 0x0A

**Table 66. Thermal Alarm Hysteresis Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:0] | THERM_HYST[7:0] | Sets the hysteresis of the over-temperature thermal alarm. 1℃ resolution. | | 00001010 | R/W |

## ADCn Hysteresis Registers

Register address: 0xC1 to 0xC6

Reset value = 0x08

**Table 67. ADCn Hysteresis Registers Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | Reserved | | | 0 | R/W |
| D[6:0] | ADCn_HYST[6:0] | Sets hysteresis of the channel ADCn alarm. The resolution is 1LSB. | | 00001000 | R/W |

# REGISTER MAPS (continued)

## DACA Clear 0 Register

Register address: 0xCA

Reset value = 0x00

**Table 68. DACA Clear 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA7_CLR | This according bit is set to '1'. The according DAC channel is forced into a clear state.<br>0 = DAC_An is kept in normal operation (default)<br>1 = DAC_An is software forced into clear state | | 0 | R/W |
| D[6] | DACA6_CLR | | | 0 | R/W |
| D[5] | DACA5_CLR | | | 0 | R/W |
| D[4] | DACA4_CLR | | | 0 | R/W |
| D[3] | DACA3_CLR | | | 0 | R/W |
| D[2] | DACA2_CLR | | | 0 | R/W |
| D[1] | DACA1_CLR | | | 0 | R/W |
| D[0] | DACA0_CLR | | | 0 | R/W |

## DACA Clear 1 Register

Register address: 0xCB

Reset value = 0x00

**Table 69. DACA Clear 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA15_CLR | This according bit is set to '1'. The according DAC channel is forced into a clear state.<br>0 = DAC_An is kept in normal operation (default)<br>1 = DAC_An is software forced into clear state | | 0 | R/W |
| D[6] | DACA14_CLR | | | 0 | R/W |
| D[5] | DACA13_CLR | | | 0 | R/W |
| D[4] | DACA12_CLR | | | 0 | R/W |
| D[3] | DACA11_CLR | | | 0 | R/W |
| D[2] | DACA10_CLR | | | 0 | R/W |
| D[1] | DACA9_CLR | | | 0 | R/W |
| D[0] | DACA8_CLR | | | 0 | R/W |

## DACA Clear 2 Register

Register address: 0xCC

Reset value = 0x00

**Table 70. DACA Clear 2 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA23_CLR | This according bit is set to '1'. The according DAC channel is forced into a clear state.<br>0 = DAC_An is kept in normal operation (default)<br>1 = DAC_An is software forced into clear state | | 0 | R/W |
| D[6] | DACA22_CLR | | | 0 | R/W |
| D[5] | DACA21_CLR | | | 0 | R/W |
| D[4] | DACA20_CLR | | | 0 | R/W |
| D[3] | DACA19_CLR | | | 0 | R/W |
| D[2] | DACA18_CLR | | | 0 | R/W |
| D[1] | DACA17_CLR | | | 0 | R/W |
| D[0] | DACA16_CLR | | | 0 | R/W |

# REGISTER MAPS (continued)

## DACA Clear 3 Register

Register address: 0xCD

Reset value = 0x00

**Table 71. DACB Clear 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA31_CLR | This according bit is set to '1'. The according DAC channel is forced into a clear state.<br>0 = DAC_An is kept in normal operation (default)<br>1 = DAC_An is software forced into clear state | | 0 | R/W |
| D[6] | DACA30_CLR | | | 0 | R/W |
| D[5] | DACA29_CLR | | | 0 | R/W |
| D[4] | DACA28_CLR | | | 0 | R/W |
| D[3] | DACA27_CLR | | | 0 | R/W |
| D[2] | DACA26_CLR | | | 0 | R/W |
| D[1] | DACA25_CLR | | | 0 | R/W |
| D[0] | DACA24_CLR | | | 0 | R/W |

## DACB Clear 0 Register

Register address: 0xCE

Reset value = 0x00

**Table 72. DACB Clear 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB7_CLR | This according bit is set to '1'. The according DAC channel is forced into a clear state.<br>0 = DAC_Bn is kept in normal operation (default)<br>1 = DAC_Bn is software forced into clear state | | 0 | R/W |
| D[6] | DACB6_CLR | | | 0 | R/W |
| D[5] | DACB5_CLR | | | 0 | R/W |
| D[4] | DACB4_CLR | | | 0 | R/W |
| D[3] | DACB3_CLR | | | 0 | R/W |
| D[2] | DACB2_CLR | | | 0 | R/W |
| D[1] | DACB1_CLR | | | 0 | R/W |
| D[0] | DACB0_CLR | | | 0 | R/W |

## DACB Clear 1 Register

Register address: 0xCF

Reset value = 0x00

**Table 73. DACB Clear 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB15_CLR | This according bit is set to '1'. The according DAC channel is forced into a clear state.<br>0 = DAC_Bn is kept in normal operation (default)<br>1 = DAC_Bn is software forced into clear state | | 0 | R/W |
| D[6] | DACB14_CLR | | | 0 | R/W |
| D[5] | DACB13_CLR | | | 0 | R/W |
| D[4] | DACB12_CLR | | | 0 | R/W |
| D[3] | DACB11_CLR | | | 0 | R/W |
| D[2] | DACB10_CLR | | | 0 | R/W |
| D[1] | DACB9_CLR | | | 0 | R/W |
| D[0] | DACB8_CLR | | | 0 | R/W |

# REGISTER MAPS (continued)

## DACA Power-Down 0 Register

Register address: 0xD0

Reset value = 0x00

**Table 74. DACA Power-Down 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA7_EN | Sets according bit to '1', enable the according DAC channel.<br>0 = DAC is powered down (default)<br>1 = DAC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[6] | DACA6_EN | | | 0 | R/W |
| D[5] | DACA5_EN | | | 0 | R/W |
| D[4] | DACA4_EN | | | 0 | R/W |
| D[3] | DACA3_EN | | | 0 | R/W |
| D[2] | DACA2_EN | | | 0 | R/W |
| D[1] | DACA1_EN | | | 0 | R/W |
| D[0] | DACA0_EN | | | 0 | R/W |

## DACA Power-Down 1 Register

Register address: 0xD1

Reset value = 0x00

**Table 75. DACA Power-Down 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA15_EN | Sets according bit to '1', enable the according DAC channel.<br>0 = DAC is powered down (default)<br>1 = DAC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[6] | DACA14_EN | | | 0 | R/W |
| D[5] | DACA13_EN | | | 0 | R/W |
| D[4] | DACA12_EN | | | 0 | R/W |
| D[3] | DACA11_EN | | | 0 | R/W |
| D[2] | DACA10_EN | | | 0 | R/W |
| D[1] | DACA9_EN | | | 0 | R/W |
| D[0] | DACA8_EN | | | 0 | R/W |

## DACA Power-Down 2 Register

Register address: 0xD2

Reset value = 0x00

**Table 76. DACA Power-Down 2 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA23_EN | Sets according bit to '1', enable the according DAC channel.<br>0 = DAC is powered down (default)<br>1 = DAC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[6] | DACA22_EN | | | 0 | R/W |
| D[5] | DACA21_EN | | | 0 | R/W |
| D[4] | DACA20_EN | | | 0 | R/W |
| D[3] | DACA19_EN | | | 0 | R/W |
| D[2] | DACA18_EN | | | 0 | R/W |
| D[1] | DACA17_EN | | | 0 | R/W |
| D[0] | DACA16_EN | | | 0 | R/W |

# REGISTER MAPS (continued)

## DACA Power-Down 3 Register

Register address: 0xD3

Reset value = 0x00

**Table 77. DACB Power-Down 3 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACA31_EN | Sets according bit to '1', enable the according DAC channel.<br>0 = DAC is powered down (default)<br>1 = DAC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[6] | DACA30_EN | | | 0 | R/W |
| D[5] | DACA29_EN | | | 0 | R/W |
| D[4] | DACA28_EN | | | 0 | R/W |
| D[3] | DACA27_EN | | | 0 | R/W |
| D[2] | DACA26_EN | | | 0 | R/W |
| D[1] | DACA25_EN | | | 0 | R/W |
| D[0] | DACA24_EN | | | 0 | R/W |

## DACB Power-Down 0 Register

Register address: 0xD4

Reset value = 0x00

**Table 78. DACB Power-Down 0 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB7_EN | Sets according bit to '1', enable the according DAC channel.<br>0 = DAC is powered down (default)<br>1 = DAC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[6] | DACB6_EN | | | 0 | R/W |
| D[5] | DACB5_EN | | | 0 | R/W |
| D[4] | DACB4_EN | | | 0 | R/W |
| D[3] | DACB3_EN | | | 0 | R/W |
| D[2] | DACB2_EN | | | 0 | R/W |
| D[1] | DACB1_EN | | | 0 | R/W |
| D[0] | DACB0_EN | | | 0 | R/W |

## DACB Power-Down 1 Register

Register address: 0xD5

Reset value = 0x00

**Table 79. DACB Power-Down 1 Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7] | DACB15_EN | Sets according bit to '1', enable the according DAC channel.<br>0 = DAC is powered down (default)<br>1 = DAC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[6] | DACB14_EN | | | 0 | R/W |
| D[5] | DACB13_EN | | | 0 | R/W |
| D[4] | DACB12_EN | | | 0 | R/W |
| D[3] | DACB11_EN | | | 0 | R/W |
| D[2] | DACB10_EN | | | 0 | R/W |
| D[1] | DACB9_EN | | | 0 | R/W |
| D[0] | DACB8_EN | | | 0 | R/W |

# REGISTER MAPS (continued)

## Monitor Power Enable Register

Register address: 0xD6

Reset value = 0x00

**Table 80. Monitor Power Enable Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:3] | Reserved | | | 00000 | R/W |
| D[2] | LT_EN | Internal Temperature Sensor Enable Bit<br>0 = Internal temperature sensor is powered down (default)<br>1 = Internal temperature sensor is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |
| D[1] | Reserved | | | 0 | R/W |
| D[0] | ADC_EN | ADC Enable Bit<br>0 = ADC is powered down (default)<br>1 = ADC is enabled<br>When powered up or reset, the default value is '0'. | | 0 | R/W |

## ADC Trigger Register

Register address: 0xE0

Reset value = 0x00

**Table 81. ADC Trigger Register Details**

| BITS | BIT NAME | DESCRIPTION | COMMENT | PORV | TYPE |
|---|---|---|---|---|---|
| D[7:1] | Reserved | | | 0000000 | R/W |
| D[0] | ADC_TRIG | Internal ADC Conversion Trigger Bit<br>Set it to '1' to trigger an ADC conversion start. Once the ADC conversion starts, the bit is set to '0' automatically. | | 0 | R/W |

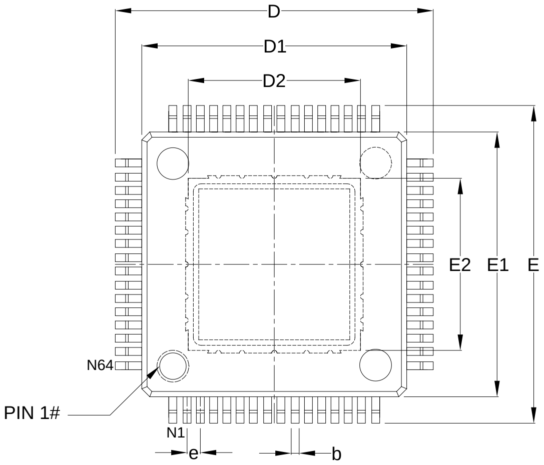
# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

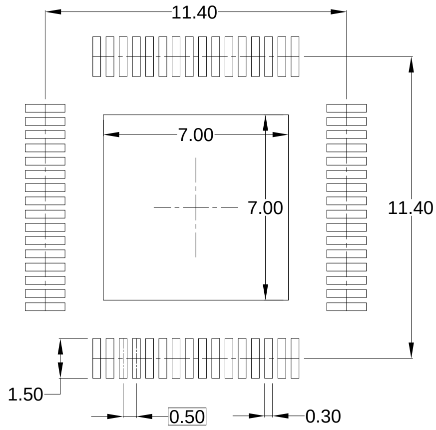
| Changes from Original (APRIL 2022) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

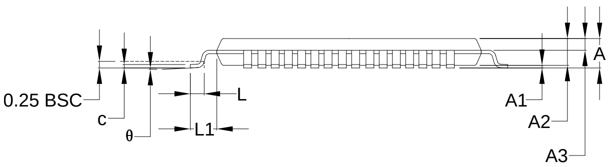
## TQFP-10×10-64L (Exposed Pad)




**TOP VIEW**




**RECOMMENDED LAND PATTERN** (Unit: mm)



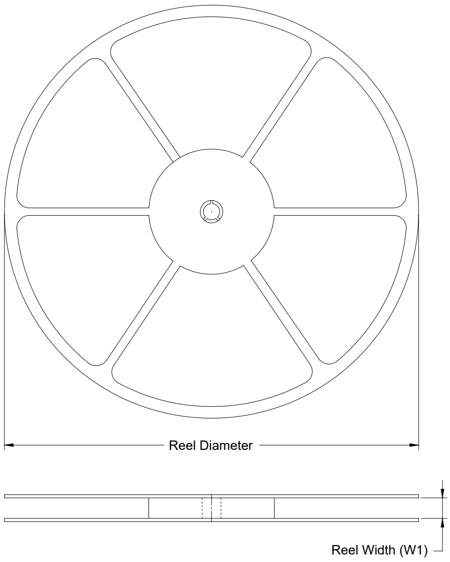

**SIDE VIEW**

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | - | - | 1.200 |
| A1 | 0.050 | - | 0.150 |
| A2 | 0.950 | 1.000 | 1.050 |
| A3 | 0.390 | 0.440 | 0.490 |
| b | 0.170 | - | 0.270 |
| c | 0.090 | 0.130 | 0.180 |
| D | 11.800 | 12.000 | 12.200 |
| D1 | 9.900 | 10.000 | 10.100 |
| D2 | 5.900 | - | 6.800 |
| E | 11.800 | 12.000 | 12.200 |
| E1 | 9.900 | 10.000 | 10.100 |
| E2 | 5.900 | - | 6.800 |
| e | 0.400 | 0.500 | 0.600 |
| L | 0.450 | - | 0.750 |
| L1 | 1.000 REF | | |
| θ | 0° | 3.5° | 7° |

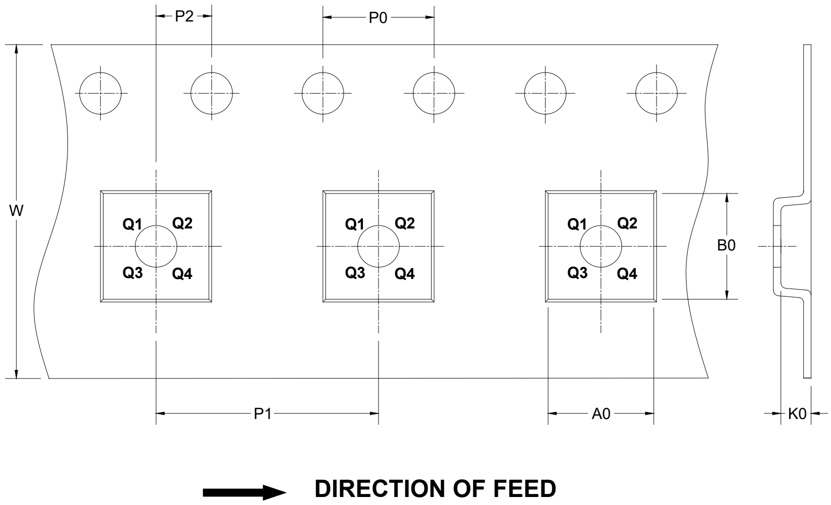
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



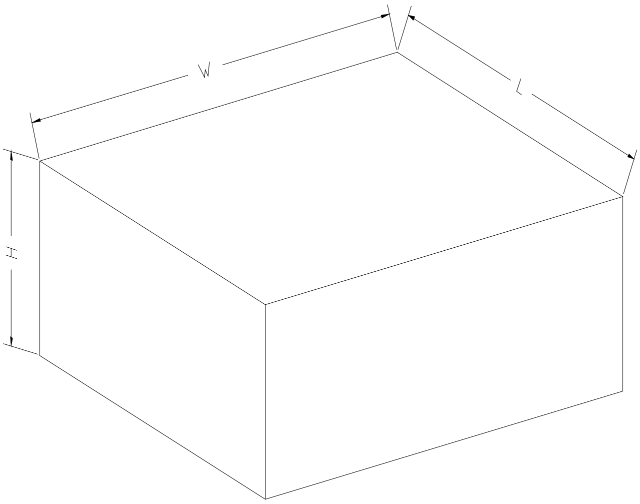

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TQFP-10×10-64L (Exposed Pad) | 13″ | 24.4 | 12.70 | 12.70 | 1.70 | 4.0 | 16.0 | 2.0 | 24.0 | Q2 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002